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# A 12-bit 50M samples/s digitally self-calibrated pipelined ADC

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**A 12-bit 50M samples/s digitally self-calibrated pipelined ADC**

by

Xiaohong Du

A thesis submitted to the graduate faculty  
in partial fulfillment of the requirements for the degree of  
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Major: Electrical Engineering

Major Professors: Marwan M. Hassoun and William C. Black

Iowa State University

Ames, Iowa

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Graduate College  
Iowa State University

This is to certify that the Master's thesis of  
Xiaohong Du  
has met the thesis requirements of Iowa State University

Signatures have been redacted for privacy

## TABLE OF CONTENTS

<b>ACKNOWLEDGEMENTS</b> . . . . .	ix
<b>ABSTRACT</b> . . . . .	x
<b>1 INTRODUCTION</b> . . . . .	1
1.1 Overview . . . . .	1
1.2 Thesis Organization . . . . .	2
1.3 Analog-to-digital Converter Architectures . . . . .	2
1.3.1 Flash converters . . . . .	2
1.3.2 Two-step flash ADC . . . . .	3
1.3.3 Successive Approximation ADC . . . . .	4
1.3.4 Oversampled ADC . . . . .	6
1.3.5 Pipelined ADC . . . . .	7
<b>2 PIPELINE ARCHITECTURE AND DIGITAL SELF-CALIBRATION</b>	9
2.1 Pipelined Architecture And Origin Of Errors . . . . .	9
2.1.1 General architecture . . . . .	9
2.1.2 1-bit-per-stage binary radix pipeline architecture . . . . .	10
2.1.3 Origin of errors and their effects . . . . .	12
2.2 Digital Self-calibration . . . . .	14
2.2.1 Digital self-calibration algorithm based on non-binary radix pipeline [Karanicolas93] . . . . .	15
2.2.2 Accuracy bootstrapped digital self-calibration algorithm . . . . .	18

2.3	Prototype Radix 1.9 1-bit-per-stage Digitally Self-calibrated Pipelined ADC	19
2.4	Conclusion . . . . .	22
<b>3</b>	<b>SYSTEM IMPLEMENTATION . . . . .</b>	<b>23</b>
3.1	System Specification And Timing . . . . .	23
3.2	Design Of The Multiplying Digital-to-analog Converter . . . . .	26
3.2.1	Sample-and-hold Nonidealities . . . . .	26
3.2.2	Multiplying digital-to-analog converter . . . . .	28
3.2.3	Operational amplifier architecture . . . . .	32
3.2.4	Simulation results of MDAC . . . . .	49
3.3	Comparator Design And Simulation Result . . . . .	49
3.4	Conclusion . . . . .	50
<b>4</b>	<b>SYSTEM SIMULATION RESULTS AND LAYOUT . . . . .</b>	<b>53</b>
4.1	System Simulation Results . . . . .	53
4.1.1	System simulation results with gain of 2 MDAC . . . . .	53
4.1.2	System simulation result with gain of 1.9 MDAC . . . . .	54
4.2	Layout Considerations . . . . .	57
4.2.1	Operational transconductance amplifier layout . . . . .	59
4.2.2	Capacitor layout . . . . .	59
4.2.3	Layout of one stage . . . . .	60
4.3	I/O Signals And Off-chip Calibration . . . . .	63
<b>5</b>	<b>CONCLUSION AND FUTURE WORK . . . . .</b>	<b>64</b>
5.1	Conclusion . . . . .	64
5.2	Power Optimization . . . . .	64
5.3	Speed Optimization . . . . .	65
	<b>APPENDIX TRANSISTOR SIZES . . . . .</b>	<b>67</b>
	<b>BIBLIOGRAPHY . . . . .</b>	<b>68</b>

## LIST OF TABLES

Table 3.1	System specification . . . . .	23
Table 3.2	Gain-boosted amplifier specification . . . . .	52
Table 3.3	MDAC specification . . . . .	52
Table 3.4	Comparator specification . . . . .	52
Table 4.1	Calculation and Measurement Results . . . . .	54
Table 4.2	I/O signals for each stage . . . . .	63
Table A.1	Folded-cascode parameters . . . . .	67
Table A.2	PMOS-boosting amplifier parameters . . . . .	67
Table A.3	NMOS-boosting amplifier parameters . . . . .	67

## LIST OF FIGURES

Figure 1.1	A flash ADC . . . . .	3
Figure 1.2	Two-step flash ADC . . . . .	4
Figure 1.3	Successive approximation ADC . . . . .	5
Figure 1.4	A binary search algorithm . . . . .	5
Figure 1.5	A simple oversampled ADC . . . . .	6
Figure 1.6	A pipelined ADC . . . . .	7
Figure 2.1	One cell of a pipelined ADC . . . . .	10
Figure 2.2	A 1-bit-per-stage radix 2 pipelined ADC . . . . .	11
Figure 2.3	Ideal residue and transfer characteristic of pipeline ADC . . . . .	12
Figure 2.4	Effect of errors on the transfer curve . . . . .	13
Figure 2.5	Residue and transfer characteristic of radix $< 2$ pipeline ADC . . . . .	16
Figure 2.6	Residue and transfer characteristic of radix $< 2$ pipeline ADC with digital calibration applied . . . . .	17
Figure 2.7	Calibration scheme proposed by karanicolas . . . . .	18
Figure 2.8	Accuracy bootstrapped digital self calibration algorithm . . . . .	19
Figure 2.9	A radix 1.9 1-bit-per-stage pipelined ADC . . . . .	20
Figure 2.10	Residue plot with effect of all principal errors . . . . .	21
Figure 3.1	Timing of pipeline ADC [Karanicolas] . . . . .	25
Figure 3.2	MX2 stage with gain of 1.9 . . . . .	25
Figure 3.3	A simplest implementation of S/H . . . . .	26

Figure 3.4	Waveform of an ideal S/H circuit . . . . .	26
Figure 3.5	A fully differential multiplying DAC . . . . .	29
Figure 3.6	Timing Diagram . . . . .	29
Figure 3.7	MDAC during different clock phases . . . . .	30
Figure 3.8	Schematic of a fully differential folded-cascode opamp . . . . .	34
Figure 3.9	small-signal equivalent circuit for folded-cascode amplifier . . . . .	34
Figure 3.10	Load of opamp in pipelined applicaiton . . . . .	35
Figure 3.11	AC response of folded-cascode amplifier: magnitude . . . . .	36
Figure 3.12	AC response of folded-cascode amplifier: phase . . . . .	36
Figure 3.13	Cascode gain stage with gain enhancement . . . . .	37
Figure 3.14	Bode plots of the original,additional and improved gain stage . . . . .	38
Figure 3.15	PMOS boosting amplifier . . . . .	39
Figure 3.16	AC response of PMOS boosting amplifier: magnitude . . . . .	40
Figure 3.17	AC response of PMOS boosting amplifier: phase . . . . .	40
Figure 3.18	NMOS boosting amplifier . . . . .	41
Figure 3.19	AC response of NMOS boosting amplifier: magnitude . . . . .	42
Figure 3.20	AC response of NMOS boosting amplifier: magnitude . . . . .	42
Figure 3.21	A gain-boosted fully differential folded-cascode amplifier . . . . .	43
Figure 3.22	AC response of gain-boosted folded-cascode amplifier: magnitude . . . . .	46
Figure 3.23	AC response of gain-boosted folded-cascode amplifier: phase . . . . .	46
Figure 3.24	Common-mode feedback circuit . . . . .	47
Figure 3.25	cm bias voltage generator . . . . .	48
Figure 3.26	Bias circuit . . . . .	48
Figure 3.27	Master current mirror . . . . .	49
Figure 3.28	Transient analysis of the MDAC . . . . .	50
Figure 3.29	Differential connection between the MDAC and comparator . . . . .	50
Figure 3.30	Schematic of the comparator . . . . .	51

Figure 3.31	Transient analysis of the comparator . . . . .	51
Figure 4.1	Top level block diagram with the interstage gain of 2 . . . . .	54
Figure 4.2	Top level simulation results with the interstage gain of 2 . . . . .	55
Figure 4.3	Top level simulation with 1.9X MDAC . . . . .	56
Figure 4.4	Reference scaling for gain of 2 and 1.9 . . . . .	57
Figure 4.5	Floorplan of the pipelined ADC . . . . .	58
Figure 4.6	Metal-sandwitch as a capacitor . . . . .	59
Figure 4.7	Common-centroid capacitor array . . . . .	60
Figure 4.8	Layout of one stage . . . . .	61
Figure 4.9	Layout of whole pipeline . . . . .	62

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## ABSTRACT

This thesis describes the different aspects of the design and implementation of a 12-bit 50M samples/s pipelined non-binary radix 1.9 analog-to-digital converter. The converter architecture is made up of 14 stages with an interstage gain of 1.9 (non-binary radix). Each stage is made of one fully differential sample-and-hold amplifier (SHA), a 1-bit sub-ADC (basically one comparator) and a 1-bit DAC. The sub-DAC functionality is rolled in as part of the SHA switch capacitor architecture which is referred to as the multiplying DAC (MDAC). The self-calibration function is performed in a cyclical fashion and the entire pipeline is used to perform the calibration for each stage. The settling time on the MDAC is about 9ns with a gain of approximately 81dB. The entire pipeline has been implemented in a digital 0.35 $\mu$ m CMOS process.

# 1 INTRODUCTION

## 1.1 Overview

Digital signal processing (DSP) has been proved to be a robust and cost effective way of signal processing. Between real world analog signals and any DSP system, an analog-to-digital interface, which is implemented by analog-to-digital converter (ADC), is needed. An increasing demand for high performance DSP system motivates an increasing demand for high-resolution, high-speed ADCs. However, it is challenging to integrate high-speed, high-resolution ADCs in low cost IC processes.

Pipelined analog-to-digital converters present advantages compared to flash, sub-range or successive approximation techniques because potentially high-resolution and high-speed can be achieved at the same time. Digital self-calibration techniques can be used in the pipeline architecture to improve the linearity and signal-to-noise ratio of the system.

The goal of this research is to implement a 12-b 50 Msamples/s digitally self calibrated pipelined ADC in a  $0.35\mu\text{m}$  Digital CMOS process. The off-chip digital self-calibration will be performed for the convenience of testing the calibration algorithm. With the help from Hui Liu, who designed the comparator and did the global routing, and Anil Tammineedi, who did the layout of the capacitor, the prototype ADC has been finished. The contributions of the author include:

- 1) Cell architecture based on 1-bit resolution per stage and non-binary radix. The radix is chosen to be 1.9 to allow 5% error budget.

2) Cell implementation focusing on the design of the MDAC and OTA. Specifically, a  $0.95V_{ref}$  is supplied externally and the minimum capacitor ratio in the MDAC is 0.1; Gain-boosting technique is used in the OTA design.

3) Overall system implementation of a pipeline of 14 stages including system timing, simulation and floorplanning.

## 1.2 Thesis Organization

This thesis is divided into five chapters. After an introduction, chapter 1 reviews several architectures of analog-to-digital converters. In chapter 2, pipelined ADCs are described in more detail, especially a 1-bit-per-stage design. The digital-calibration algorithm based on a non-binary radix architecture is also discussed. The circuit implementation of the pipelined ADC is presented in chapter 3, focusing on the design of a multiplying digital-to-analog converter which is the combination of the sample-and-hold amplifier, the subtracter and the sub-DAC. The system simulation results are shown in chapter 4 as well as the layout consideration. Chapter 5 will describe conclusions and some future work.

## 1.3 Analog-to-digital Converter Architectures

### 1.3.1 Flash converters

The flash architecture [Johns97][Cline95] is the most straightforward way to implement the analog-to-digital conversion. It is also fundamentally the fastest architecture since it utilizes fully parallelism. Figure 1.1 shows a block diagram of a n-bit flash ADC. The architecture is easy to understand. A n-bit flash ADC consists of an array of  $2^n - 1$  comparators, a resistor ladder generating  $2^n - 1$  reference values and a decoder. Each of the comparators samples the input signal and makes decision whether or not the input

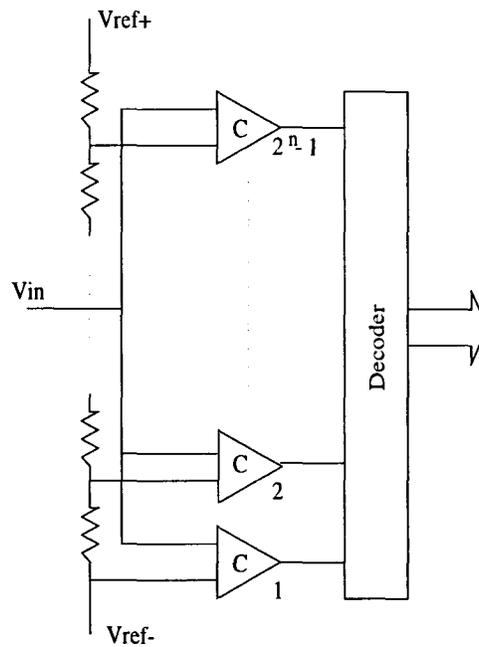


Figure 1.1 A flash ADC

is greater or less than the corresponding reference voltage. The set of  $2^n$  comparator output will send into a decoder and get a  $n$ -bit digital code.

Flash ADCs are fast because the comparators all operate in parallel. However, flash ADCs require a large number of hardware,  $2^n$  comparators, which take up a large area and very power hungry. In addition, flash ADCs are very sensitive to comparator offsets. A  $n$ -bit application requires the comparator offset less than  $1/2^n$  of the full signal swing, which is very small for high-resolution. Due to these two drawbacks, ADCs with resolution higher than 8-bit seldom use the flash architecture.

### 1.3.2 Two-step flash ADC

Figure 1.2 illustrates the structure of a two-step flash ADC. It is made up of two stages, each containing a flash ADC. The conversion takes two steps. During the first step, the first flash ADC performs a coarse quantization on the input signal and determines the most significant bits of the digital output word. The digital output is

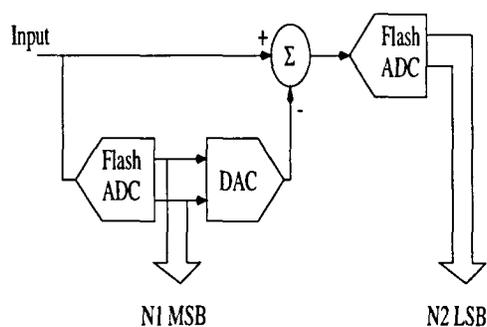


Figure 1.2 Two-step flash ADC

reconverted to analog value by a digital-to-analog converter. Then the input was subtracted from the output of DAC, the residue of the subtraction is then passed down for fine quantization to get the least significant bits.

Compared to a simple flash ADC, the advantage of this architecture is fewer comparators and less sensitive to the comparator offset. Although the conversion time is one cycle longer, it is still very fast.

### 1.3.3 Successive Approximation ADC

The successive approximation method is commonly used for fast and highly accurate ADCs [Plassche94]. The advantage of successive approximation ADCs is their little hardware requirement. An example of successive approximation ADCs is shown in Figure 1.3. It only consists of a sample-and-hold circuit, a comparator, a DAC, and a digital logic circuit, often referred to as the successive approximation register (SAR), controlling the DAC.

Successive approximation architecture is also known as a binary search ADC because it applies a binary search algorithm to determine the closest digital word to match an input signal. The algorithm is illustrated in Figure 1.4 [Johns97]. The operation of the successive approximation ADC is as follows. The control logic sets the initial value of DAC to be zero. The input signal is taken by the sample-and-hold circuit. Here the

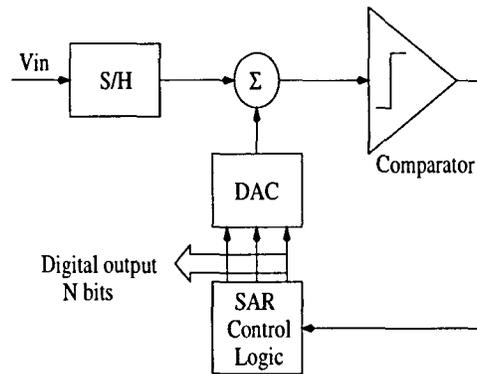


Figure 1.3 Successive approximation ADC

input signal is signed, i.e. it can either positive and negative. Since the initial output of DAC is zero, the result of the subtraction is the input sample. The comparator decides whether the input is greater or less than zero and generates a MSB digital signal which instructs the control logic to either increase or decrease the DAC output by half the reference voltage. And the DAC output is subtracted again from the input sample, and the comparator will produce the second MSB until the desired resolution is achieved.

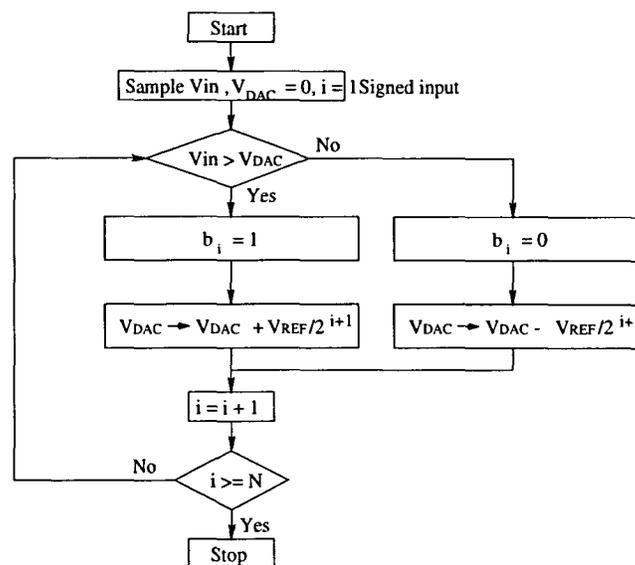


Figure 1.4 A binary search algorithm

### 1.3.4 Oversampled ADC

The oversampled ADC architecture is another architecture that is capable of achieving high-resolution with relatively little hardware, and it is widely used for audio, geophysical and other low frequency applications. Presently, the highest resolution ADCs use oversampling technique[Cline95]. A simple oversampled ADC is shown in Figure 1.5.

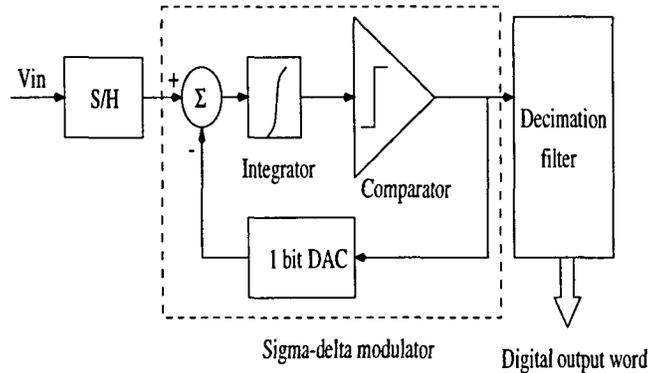


Figure 1.5 A simple oversampled ADC

The operation of oversampled ADCs is based on a sigma-delta modulator which includes a subtracter, an integrator, a comparator as the quantizer and 1-b DAC which reconstructs the analog signal. The modulator repeatedly samples the input and performs a one-bit quantization of the error between the signal and the estimation of the signal. By sampling the signal many times, the quantization errors and noise are averaged out, thus the dynamic range of the ADC can be improved. In this simple example, 1-bit ADC and DAC is used. However, to relax the oversampling ratio required, multi-bit quantizer and reconstruction circuits in the sigma-delta modulator can be used although the nonlinearity of the multi-bit digital-to-analog converter restricts the resolution of the system.

### 1.3.5 Pipelined ADC

The concept of pipelining often used in digital circuits to achieve higher throughput can also be applied in the analog domain. Figure 1.6 shows the diagram of a pipelined ADC [Cline94][Lin91][Kim96] with  $N$  stages. Each of the pipelined stages consists of a sample-and-hold circuit, a low-resolution flash sub-ADC, a low-resolution sub-DAC, a subtractor and an interstage amplifier. To begin the conversion, the input is sampled and held. The held signal is converted into a digital code, maybe one bit or multiple bits, by the first stage sub-ADC. Then the first stage sub-DAC converts the digital code back into analog signal which is subtracted from the held signal. The difference between the DAC output and the held input is the residue output of first stage. After amplified by the interstage gain, the residue is sampled by the second stage. The sub-ADC in the second stage also produce a digital code. The process is repeated until the input hit the last stage. The outputs of all the stages are combined into the digital output in an output register.

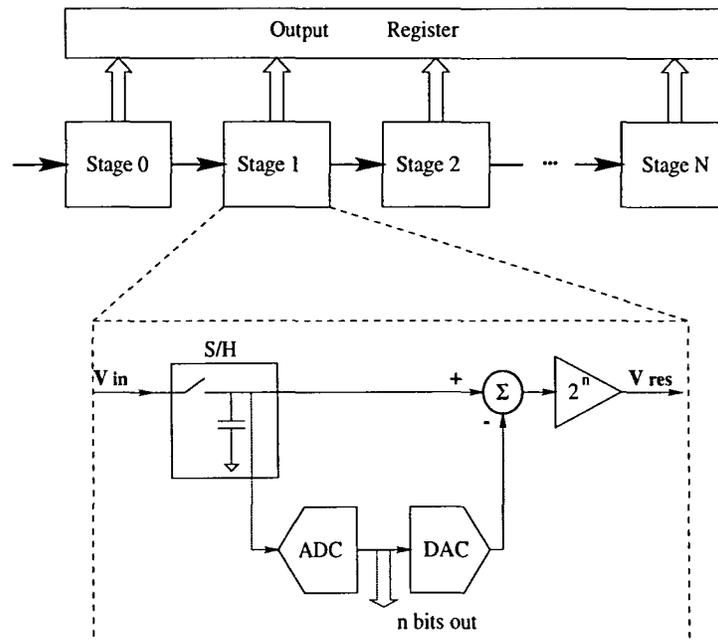


Figure 1.6 A pipelined ADC

By using a sample-and-hold circuit, each stage of pipeline can process a new sample as long as its residue is sampled by the next stage. Thus, the throughput is independent of the number of stages in the pipeline which allows the pipelined ADC to operate at high-speed. Compared to the flash architecture, the pipeline ADC architecture only requires linear growth in hardware for increasing resolution instead of exponential growth, which means dramatic die area could be saved when the resolution is high. In general, pipelined ADCs are suitable for high-speed and high-resolution application.

## 2 PIPELINE ARCHITECTURE AND DIGITAL SELF-CALIBRATION

In this chapter, we will discuss the pipelined analog-to-digital converter in more detail. The error sources and their effects on the transfer function of the system are examined as well. After discussing digital self-calibration schemes, we will present the prototype non-binary radix digitally self-calibrated pipelined ADC.

### 2.1 Pipelined Architecture And Origin Of Errors

#### 2.1.1 General architecture

The typical structure of pipelined ADCs has already been introduced in Chapter 1. A pipelined ADC consists of a number of stages. Each stage of the pipeline will resolve some segment, which can be one bit or more, of the digital output word.

Figure 2.1 shows a general stage [Lin91] for a pipelined ADC which includes a sample-and-hold circuit, a  $n$ -bit sub-ADC, a  $n$ -bit sub-DAC, a subtracter, and an interstage gain amplifier. The sample-and-hold circuit and the interstage gain amplifier can be combined into a sample-and-hold amplifier (SHA).

The ideal output of the stage  $V_{res}$  is

$$V_{res} = 2^n V_{in} - V_{DACout} \quad (2.1)$$

The most basic architectural characteristic for a pipelined ADC is the individual stage resolution, which is the integer  $n$  shown in Figure 2.1. It determines the number of stages

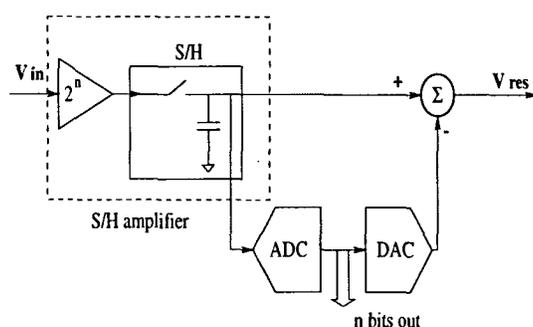


Figure 2.1 One cell of a pipelined ADC

required to obtain the total resolution and sets the value of the interstage gain. For our high-speed application which requires a conversion rate of 50M Samples/s, we would prefer the minimum stage resolution which is 1. The reason for that is: minimizing the stage resolution corresponds to minimizing the interstage gain, which, in turn, maximizes the bandwidth since the gain-bandwidth product is limited in any technology [Lewis92] because the intrinsic  $g_m$  of a transistor is limited in any technology.

Another big advantage of 1-bit-per-stage architecture is its simplicity. We will see in the next section.

### 2.1.2 1-bit-per-stage binary radix pipeline architecture

Figure 2.2 shows a 1-bit-per-stage radix 2 pipelined ADC. The pipeline begins with a front-end gain-of-1 sample-and-hold (SH) stage and is followed by multiply-by-two (MX2) stages. Each MX2 stage has an analog input and a 1-bit digital input as well as an analog output and a 1-bit digital output. The structure of MX2 stage is rather simple. The 1-bit flash sub-ADC is simply a comparator. The sub-DAC, the subtracter, and the SHA can be combined into one switch-capacitor block called multiplying digital-to-analog converter (MDAC).

Figure 2.3a shows a 8-b example of 1-bit-per-stage radix 2 pipeline ADC. The first SH stage consists of a front-end gain-of-1 SHA and a comparator monitoring the output

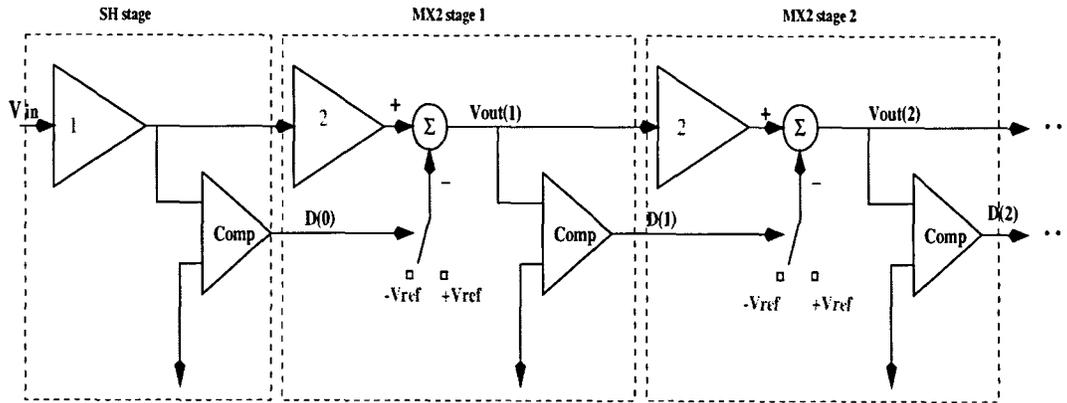


Figure 2.2 A 1-bit-per-stage radix 2 pipelined ADC

of SHA. If the input is positive, the output will be 1 otherwise it will be zero. MX2 stage 1, followed by 6 more MX2 stages, is the stage under examination and its inputs are the outputs from the preceding SH stage. Assuming all stages are ideal, the residue output of MX2 stage 1, as a function of inputs of the stage, can be written as

$$V_{out} = 2V_{in} - V_{ref} \quad \text{if } D_{in} = 1 \quad (2.2)$$

$$V_{out} = 2V_{in} + V_{ref} \quad \text{if } D_{in} = 0 \quad (2.3)$$

And the residue plot is shown in Figure 2.3b.

The digital word  $X$  is composed of bits  $D(1)D(2)...D(7)$  and is therefore the quantized representation of the residue output of MX2 stage 1. The digital output  $D_{in}:X$  is the quantized representation of  $V_{in}$  and is plotted as a function of  $V_{in}$ , resulting in an ideal linear transfer characteristic as shown in Figure 2.3c.

However, the components in the MX2 stage are nonideal and they are the main error sources which will affect the residue output and degrade the transfer characteristic of the pipelined ADC.

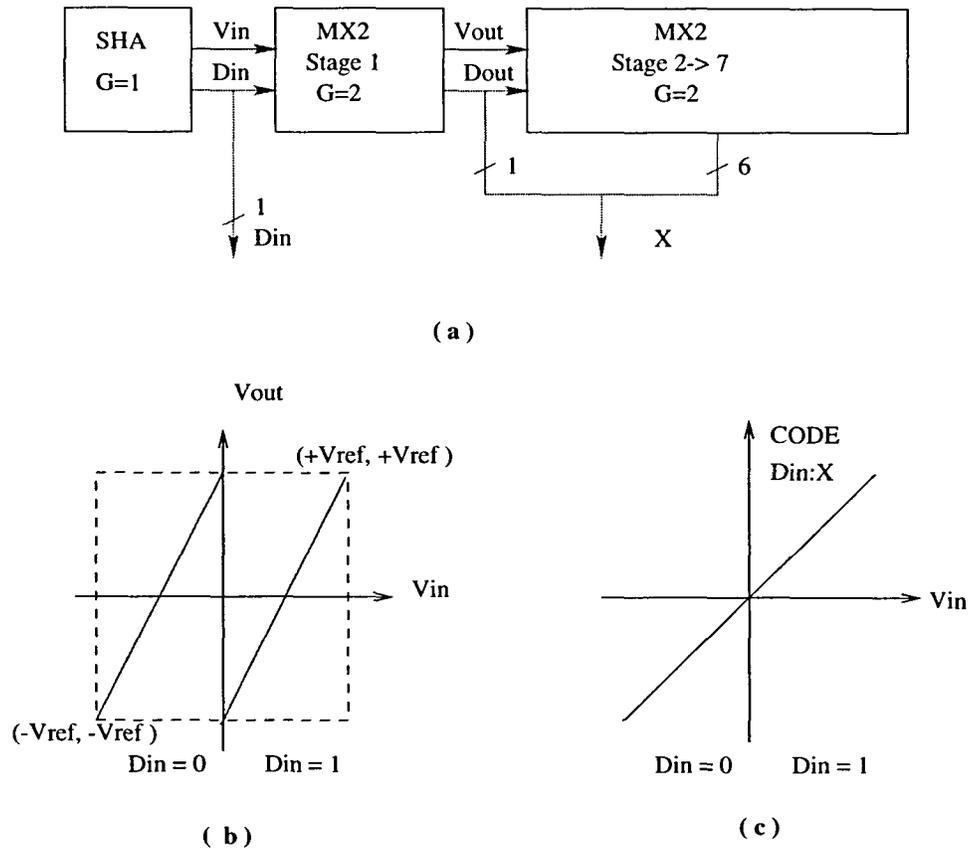


Figure 2.3 Ideal residue and transfer characteristic of pipeline ADC

### 2.1.3 Origin of errors and their effects

These errors can be recognized as errors introduced by the switched-capacitor block, which include charge injection and capacitor mismatch, comparator offset, and reference level error.

Figure 2.4 shows the ideal residue plot and the effects of principal errors on the residue plot [Karanicolas93]. Generally if the absolute value of the residue exceeds  $V_{ref}$ , missing decision levels will occur. This is because the remaining pipeline stages are saturated so the output code does not change at all for the corresponding analog input range. On the other hand, if the maximum absolute value of the residue does not reach  $V_{ref}$ , missing codes will occur since the full input range of the remaining pipeline stages is not accessed.

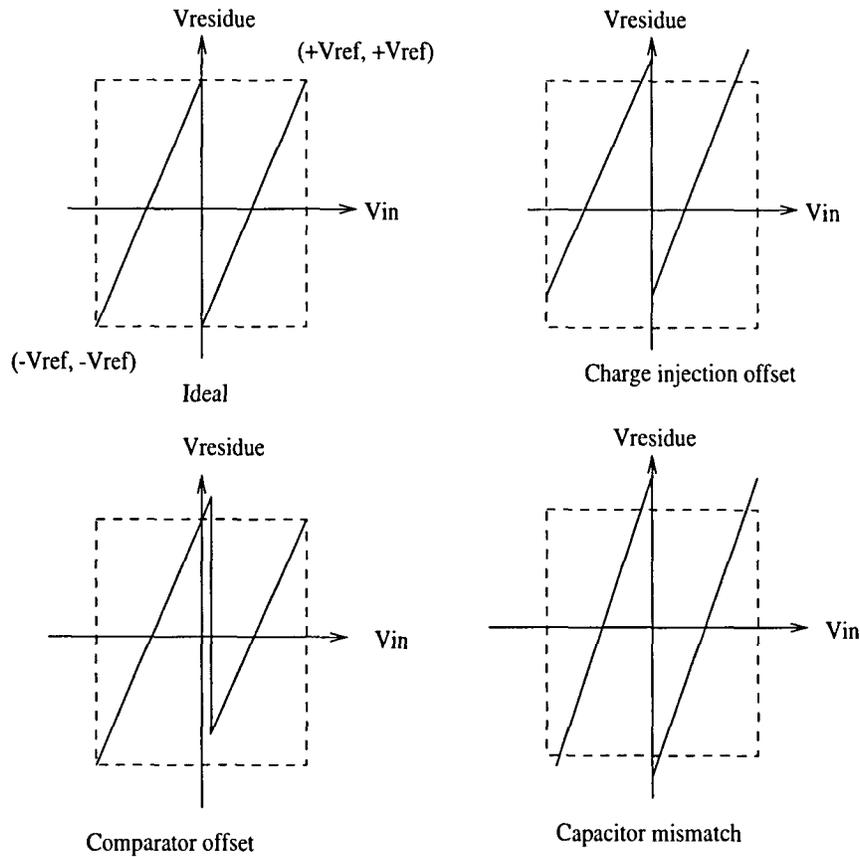


Figure 2.4 Effect of errors on the transfer curve

### 2.1.3.1 Charge injection offset

Charge injection offset causes a vertical shift of the residue plot [Karanicolas93]. The shift can be positive as well as negative, but only positive shift is shown for simplicity. Taking the 8-bit ADC shown in Figure 2.3a as an example, ideally when  $V_{in} = 0$  or  $V_{ref}$ , the residue output  $V_{out}$  will reach  $V_{ref}$  and the corresponding digital code  $X$  will be “1111111”. With a positive charge injection offset, the residue can exceed the reference boundary when the input  $V_{in}$  is either less than zero, say  $V_1$ , or less than  $V_{ref}$ , say  $V_2$ . Thus in the range  $V_1 < V_{in} < 0$  and  $V_2 < V_{in} < V_{ref}$ ,  $X$  remains “1111111” which results in missing decision levels.

Charge injection offset can also lead to missing codes when the input is either positive and near the major transition point or negative and near the minimum input voltage

$-V_{ref}$  since there is a gap from the minimum output to the reference boundary and the digital code X never goes down to “000000”.

### 2.1.3.2 Comparator offset

Comparator offset causes a shift of the major transition point since the threshold of the comparator is shifted. This leads to the residue exceeding the reference boundary as well as a gap to the reference boundary. Hence, missing decision levels and missing codes happen again.

### 2.1.3.3 Capacitor mismatch

Finally, capacitor mismatch can result in the gain either being greater or less than 2. In the former case, the residue will exceed the reference boundary and missing decision levels happen. In the latter case, the residue will have a gap from the residue extrema to the reference boundary near the major transition point and missing codes occur.

## 2.2 Digital Self-calibration

To minimize the errors discussed above, high-precision components are usually required in traditional ADC approaches, which are not compatible with low cost, MOS IC processes. Thus the use of calibration techniques is important to eliminate the need for high-precision matching.

Calibration is the process of measuring the deviation of the real transfer characteristics from the ideal characteristic and tuning the instrument to reduce the errors. Self-calibration is the process of calibration by using the component itself to measure its own errors and it can be done either in analog domain or in digital domain. Although, in general, analog calibration does not need extra clock cycles for calibration, usually capacitor trimming or error averaging is needed which adds complexity to the analog

circuitry. Digital calibration is performed in the digital domain at the price of more digital circuitry which is easier to implement in a digital CMOS process, which is our target here. Therefore digital self calibration is preferable to analog calibration in our application.

Section 2.2.1 covers a digital self-calibration technique based on a radix  $< 2$  and 1-bit-per-stage conversion algorithm presented in [Karanicolas93]. To achieve more accuracy of the calibration results, [Ray97] proposed an improved digital self-calibration algorithm by applying accuracy bootstrapping technique [Soenen95]. It will be covered in section 2.2.2. This thesis implements a digital self-calibration algorithm which is the combination of these two algorithms.

### **2.2.1 Digital self-calibration algorithm based on non-binary radix pipeline [Karanicolas93]**

In section 2.1.2, we learned the origin of errors and their effects on the transfer characteristic of a radix 2 pipeline. When the output of any stage exceeds the reference boundary, missing decision levels happen, which cannot be eliminated by digital calibration alone. On the other hand, when the output extrema forms a gap to the reference boundary, missing codes happen and it can be eliminated by digital self-calibration. The key for employing a radix  $< 2$  pipeline is to use a nominal gain less than 2, such that the output of each stage never exceed the reference boundary even with the presence of errors. The missing codes resulting from gain less than 2 can be calibrated out as will be illustrated later in this section. The ADC shown in Figure 2.5a is the same as the one shown in Figure 2.3a except the stage after the SH stage has a gain of less than 2. Again all the stages are assumed ideal, the residue and transfer characteristics are shown in Figure 2.5b and 2.5c.

The residue plot of MX2 stage 1 with gain reduction and zero comparator offset as well as transfer characteristic are shown in Figure 2.5b and 2.5c. It can be seen that X

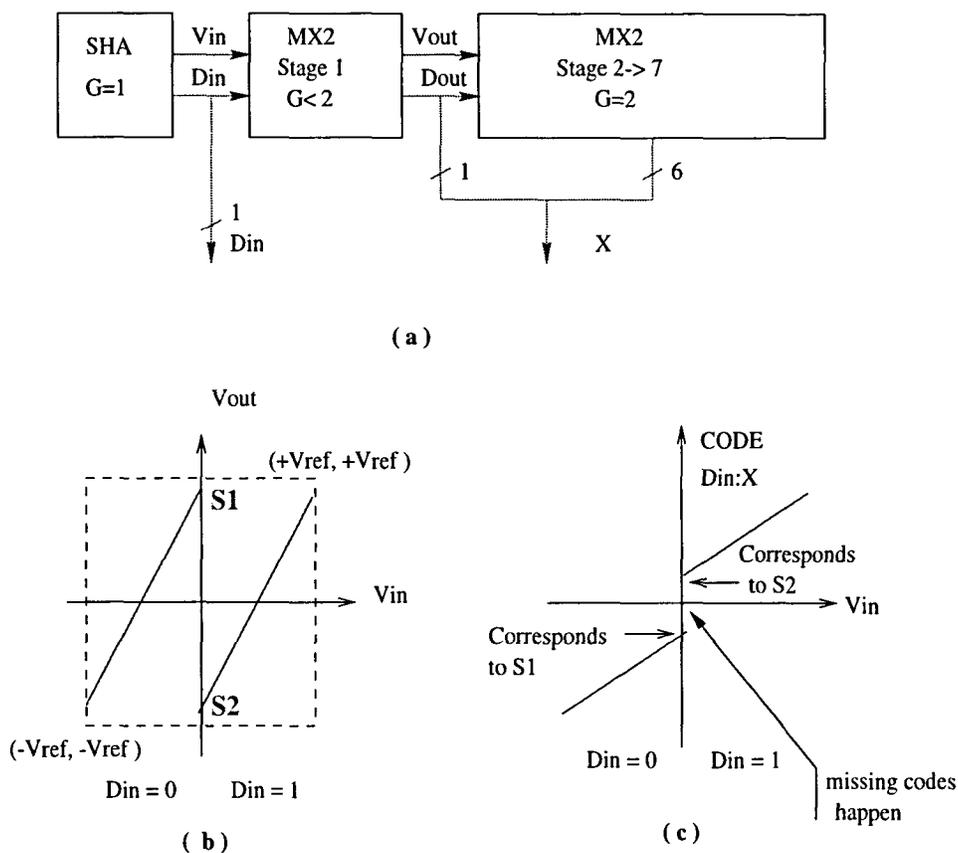


Figure 2.5 Residue and transfer characteristic of radix  $< 2$  pipeline ADC

does not reach the maximum or minimum value possible because the gain is reduced for MX2 stage 1. Thus  $D_{in}:X$  has missing codes at the major carry transition point.

The same structure as before but with digital calibration logic applied is shown in Figure 2.6. In this figure, MX2 stage 1 is being digitally calibrated. The outputs  $D$  and  $X$  are presented to the digital calibration logic system along with two calibration constants  $S1$  and  $S2$  determined for stage 1. The two quantities  $S1$  and  $S2$  are identified on the residue plot and correspond to the quantized representation of  $V_{out}$ , when  $V_{in} = 0$ , with  $D = 0$  and  $D = 1$  respectively.

To determine  $S1$ , the analog input of MX2 stage 1 is set to zero and the input bit is forced to zero, the quantity  $X$  in this case is  $S1$ . In an analogous manner, the analog input is still zero but the input bit is forced to 1,  $S2$  is determined.

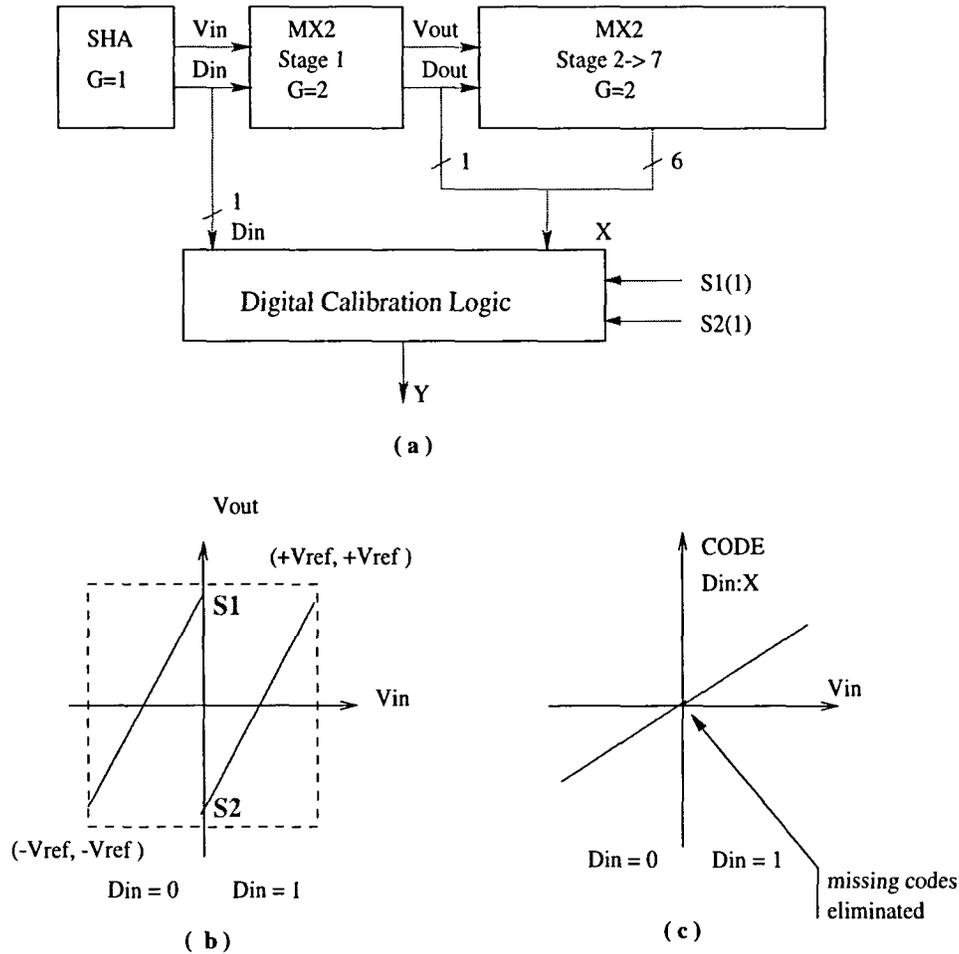


Figure 2.6 Residue and transfer characteristic of radix  $< 2$  pipeline ADC with digital calibration applied

The digital self-calibration algorithm can now be stated as:

$$Y = X, \quad \text{if } D = 0 \quad (2.4)$$

$$Y = X + S1 - S2, \quad \text{if } D = 1 \quad (2.5)$$

This transform ensures that the output code  $Y$  with  $V_{in} = 0$  is equal for  $D_{in} = 0$  and  $D_{in} = 1$ , thus missing codes shown in Fig 2.5c are eliminated as seen from Figure 2.6c.

A 15-bit 1-Msample/s digitally self-calibrated pipelined ADC based on the calibration algorithm described above was demonstrated [Karanicolas93]. The non-binary gain is set to 1.93 to relax the comparator offset requirement, which means up to 1.75% of

$V_{ref}$  can be corrected by calibration (a mathematical derivation of 2.5% of  $V_{ref}$  for the case of radix 1.9 is shown in next section). To provide decision level redundancy for a 15-bit resolution, 18 stages are used including an input SH stage. The block diagram is shown in Figure 2.7 and the calibration is first applied on MX2 stage 11 by determining the calibration constants  $S1$  and  $S2$  same as shown in Figure 2.6. After the 11th stage is done, the calibration goes to higher level stage which is MX2 stage 10 in a similar way. Same procedure continues up to the first MX2 stage.

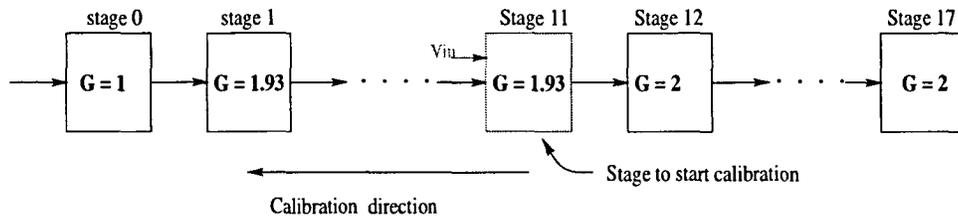


Figure 2.7 Calibration scheme proposed by karanicolas

### 2.2.2 Accuracy bootstrapped digital self-calibration algorithm

In the digital self-calibration algorithm discussed above, when a stage is being calibrated, only those stages which are downstream of the calibration stage are being used for measuring the two calibration constants:  $S1$  and  $S2$ . Thus,  $S1$  and  $S2$  have low precision. For example, for stage 11, only stages 11 through 17 are used to measure the calibration constants, and thus  $S1$  and  $S2$  have 7-bit accuracy. In addition, the gain-of-2 MX2 stages 12 ~ 17 are not calibrated at all. These are major drawbacks of the calibration scheme. To make the calibration result more accurate, [Ray97] proposed a digital calibration algorithm that uses all stages of the pipeline cyclically, similar to the scheme reported in accuracy bootstrapping algorithm [Soenen95], to determine the calibration constants  $S1$  and  $S2$  for each stage to achieve more precision on  $S1$  and  $S2$ . Figure 2.8 shows the calibration scheme.

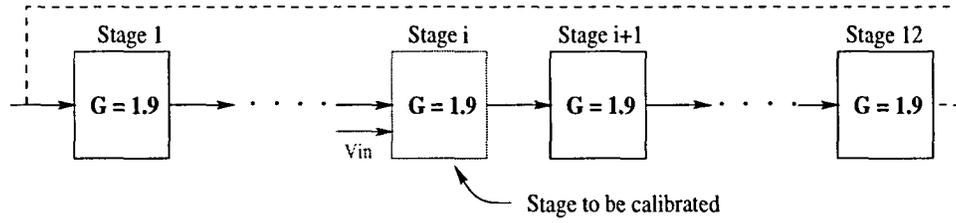


Figure 2.8 Accuracy bootstrapped digital self calibration algorithm

For a 12-bit pipelined ADC, the last stage (stage 12) is first calibrated. Stages 1 through 11, which can be taken as downstream stages of stage 12 in a cyclic manner, are used to measure the calibration constants  $S_1$  and  $S_2$  of stage 12. Then stage 11 is calibrated using stages 12, 1 through 10 in a similar way. The calibration procedure continues until the first MX2 stage is calibrated. In general, to calibrate stage  $i$ , the pipeline made up of stages  $i+1$  through 12, 1 through  $i$ , is used to measure the calibration constants  $S_1$  and  $S_2$  to achieve maximum accuracy. Note that in this case, stage  $i+1$  is the first stage of the measuring pipeline.

### 2.3 Prototype Radix 1.9 1-bit-per-stage Digitally Self-calibrated Pipelined ADC

Figure 2.9 presents a proposed pipelined ADC based on non-binary radix 1.9, 1-bit-per-stage design. The interstage gain is chosen to be 1.9 and the residue of a MX2 stage would be

$$V_{out} = 1.9V_{in} - 0.95V_{ref} \quad \text{if } D_{in} = 1 \quad (2.6)$$

$$V_{out} = 1.9V_{in} + 0.95V_{ref} \quad \text{if } D_{in} = 0 \quad (2.7)$$

To explain the reason to choose 1.9 radix, we need to analyze the residue output mathematically. Figure 2.9 shows the residue plot with the effect of all principal errors. Calibration constants  $S_1$  and  $S_2$  are also shown on the plot. Assume there is a gain error  $\delta A$  caused by capacitor mismatch, a relative reference voltage error  $\delta D_0$  associated with

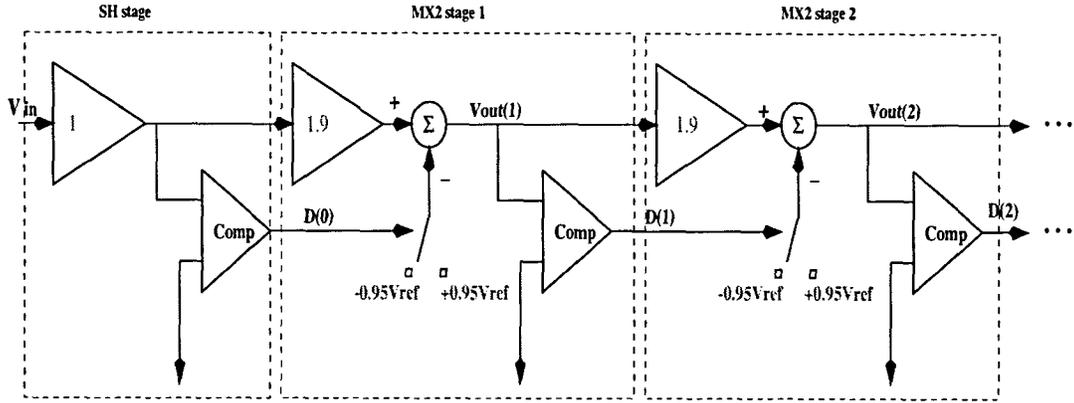


Figure 2.9 A radix 1.9 1-bit-per-stage pipelined ADC

$0.95V_{ref}$ ,  $D0$ , and  $\delta D1$  associated with the  $-0.95V_{ref}$ ,  $D1$ . Equations 2.6 and 2.7 can be rewritten as

$$V_{out} = (1.9 + \delta A)V_{in} + 0.95V_{ref}(1 + \delta D0) \quad \text{if } D_{in} = 0; \quad (2.8)$$

$$V_{out} = (1.9 + \delta A)V_{in} - 0.95V_{ref}(1 + \delta D1) \quad \text{if } D_{in} = 1; \quad (2.9)$$

To prevent the residue from exceeding the reference boundary, the output must always satisfy:

$$-V_{ref} \leq V_{out} \leq V_{ref} \quad (2.10)$$

Let us first assume there are no comparator offsets, when  $V_{in} = -V_{ref}$ , from equation 2.8,

$$V_{out} = -(1.9 + \delta A)V_{ref} + 0.95V_{ref}(1 + \delta D0) \geq -V_{ref} \quad (2.11)$$

Accordingly we have

$$0.95V_{ref}\delta D0 \geq -0.05V_{ref} \quad (2.12)$$

which means up to 5% of the reference error can be tolerated. When  $V_{in} = V_{ref}$ , similarly we have

$$0.95V_{ref}\delta D1 \leq 0.05V_{ref} \quad (2.13)$$

Letting  $V_{in} = 0$  in equation 2.8, we can determine  $S1$ . Similarly  $S2$  can be determined from equation 2.9. Hence,  $S2$ ,

$$S1 - S2 = 0.95V_{ref}(2 + \delta D0 + \delta D1) \quad (2.14)$$

With the presence of the comparator offset, the calibration constants would be  $S1'$  and  $S2'$ . Since comparator offset just causes the shift of the major transition point, it is obvious that  $S1 - S2 = S1' - S2'$ , which means the comparator offset can be ignored as long as the residue output never exceeds the reference boundary.

Let us first consider the case of positive comparator offset  $V_{os}$  as shown in Figure 2.10,  $S1'$  is prone to exceed the reference boundary:

$$S1' = 0.95V_{ref}(1 + \delta D0) + (1.9 + \delta A)V_{os} \quad (2.15)$$

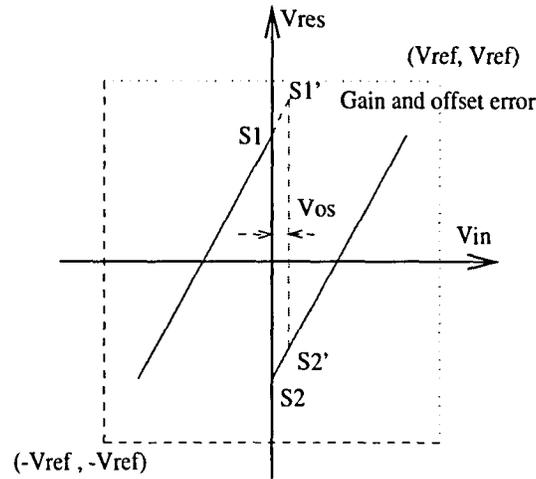


Figure 2.10 Residue plot with effect of all principal errors

In order to avoid missing decision level, i.e. prevent overrange,  $S1'$  needs to satisfy

$$S1' < V_{ref} \quad (2.16)$$

therefore,

$$0.95V_{ref}\delta D0 + V_{os}(1.9 + \delta A) \leq 0.05V_{ref} \quad (2.17)$$

Which means the total error budget would be 5% of  $V_{ref}$ . Neglecting all other errors, the comparator offset requirement can be relaxed to be slightly over 2.5% of  $V_{ref}$ .

In the other case, where  $V_{os}$  is negative, we have

$$S2' = -0.95V_{ref}(1 + \delta D1) - (1.9 + \delta A)|V_{os}| \quad (2.18)$$

to prevent underrange, we have similar conclusion:

$$0.95V_{ref}\delta D1 + (1.9 + \delta A)|V_{os}| \leq 0.05V_{ref} \quad (2.19)$$

## 2.4 Conclusion

In this chapter, the advantage of a 1-bit-per-stage design for pipelined ADCs is first discussed. After the description of the effects of the main error sources, the digital self-calibration algorithm, which is the combination of the algorithms reported in [Karanicolas93] and [Soenen95], was presented. This thesis proposed a digitally self-calibrated pipelined ADC based on a 1-bit-per-stage and non-binary radix design. The contribution of the author is that the non-binary radix is chosen to 1.9 instead of previously reported 1.93 to allow more error budget. In the next chapter, the implementation of the proposed ADC will be discussed.

### 3 SYSTEM IMPLEMENTATION

In the previous chapter, we determined the architecture of our prototype pipelined ADC and described the digital calibration algorithm. In this chapter, the implementation of the pipelined ADC is presented which is the main contribution of this thesis.

#### 3.1 System Specification And Timing

This design is targeting at a 12-b 50M samples/s pipelined ADC using 0.35 $\mu$ m CMOS digital process. It would be a low voltage design since the power supply will be 3.3V (-1.65V - 1.65V). The specification of the ADC is listed in Table 3.1.

Table 3.1 System specification

Resolution	12-bit
Sampling freq.	50M
Dynamic range	$\pm 0.9V$
Power supply	3.3V
Power dissipation	462mW

As shown in Figure 2.9, our prototype ADC is a radix 1.9 1-bit-per-stage digitally self-calibrated pipelined ADC. The pipeline starts with a front-end sample-and-hold stage, the digital output of this stage will be the MSB (most significant bit) of the digital output word. The analog output and digital output of the SH stage are fed into the first multiply-by-two (MX2) stage which is followed by 13 identical MX2 stages. Instead of 2, the gain of the MX2 stages is set to 1.9 to allow about 5% of dynamic range as the error budget.

In a pipelined ADC, the various stages of the pipeline operate concurrently. At any instant, while the first stage processes the current input sample, the second stage processes the amplified residue of the previous input sample from the first stage. The basic timing of a pipeline ADC is shown in Figure 3.1 [Karanicolas]. Two nonoverlapping clocks  $\Phi_1$  and  $\Phi_2$  are used.

1) When  $\Phi_1$  is high, the sample-and-hold amplifier (SHA) is tracking the input. At the end of  $\Phi_1$ , the analog input is sampled.

2) When  $\Phi_2$  is high, the SHA switches to the amplify mode and its output is presented to the input of MX2 stage 1.

3) When  $\Phi_2$  goes low, the analog output of the SHA is sampled by MX2 stage 1, and the comparator monitoring the output of the SHA is strobed and the first digital bit is determined and ready to be the digital input of the MX2 stage 1.

This process will continue until the input signal has reached the end of the pipeline. The throughput of the pipeline ADC is the period of the clock since each stage is handling a new data every clock cycle. For 50Ms/s application, the clock period is 20ns. The comparator of MX2 stage 1 will make decision 10ns later than the comparator of SHA, if we assuming 50% duty cycle. Therefore, the latency will be  $12 \times 10\text{ns}$ , i.e. 120ns.

The front-end sample-and-hold stage is not covered by this thesis, hence our focus will be the first MX2 stage since the the first stage needs to have 11-bit resolution while the resolution requirement can be relaxed going down the stream. The last stage only needs to have one-bit resolution.

Figure 3.2 shows a block diagram of MX2 stage with gain of 1.9. A MX2 stage consists of a sample-and-hold amplifier of gain of 1.9, a 1-bit sub-DAC, a subtracter and a comparator as the flash 1-bit ADC. For simplicity, a single-ended version is shown in Figure 3.2, although the system is fully differential to improve power supply rejection ratio and minimize the even harmonic distortion.

By using switched capacitor techniques, the sub-DAC, subtracter and SHA all share a

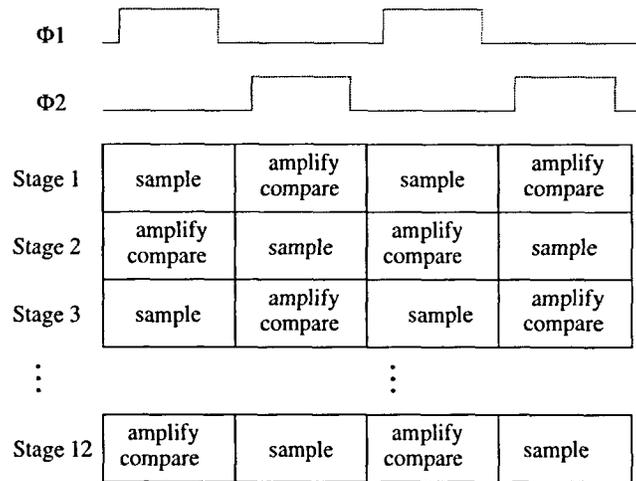


Figure 3.1 Timing of pipeline ADC [Karanicolas]

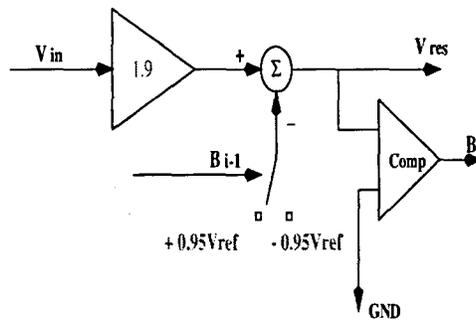


Figure 3.2 MX2 stage with gain of 1.9

common capacitor array and their functions are combined in a multiplying DAC (MDAC) [Lewis92]. The fundamental accuracy of the ADC is limited by the accuracy of the multiplying DAC which is determined by the accuracy of the sample-and-hold amplifier. For a 12b/50M application, careful circuit design is necessary. In section 3.2, we will present the design of MDAC and simulation results, and after that we will describe the comparator design.

## 3.2 Design Of The Multiplying Digital-to-analog Converter

Before going into detailed circuit design, let us go over nonidealities in sample-and-hold circuit. In the later sections, the design of the MDAC and its sub-blocks will be presented as well as the simulation results.

### 3.2.1 Sample-and-hold Nonidealities

The function of a sample-and-hold circuit is to track the analog input and to sample the input at an instant and hold the value for the next stage. The simplest implementation of SH circuits is a MOS switch with a capacitor load as shown in Figure 3.3. The ideal waveform is shown in Figure 3.4.

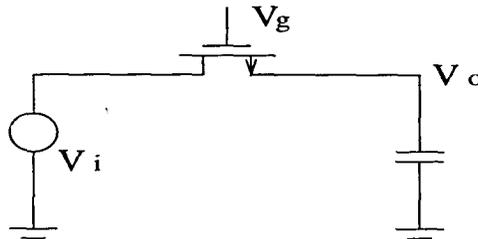


Figure 3.3 A simplest implementation of S/H

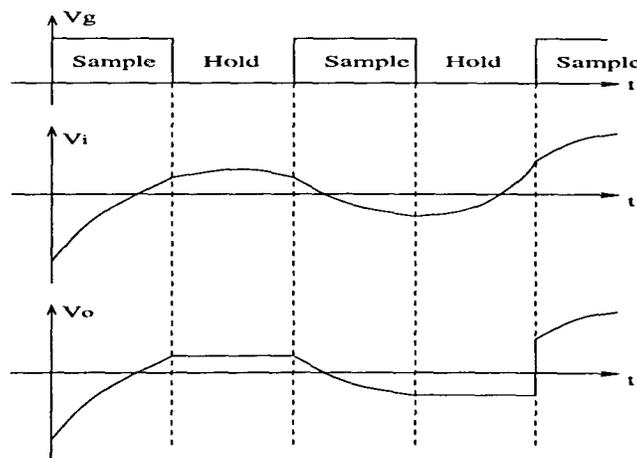


Figure 3.4 Waveform of an ideal S/H circuit

However, there are some nonidealities associated with the elements of the SH circuit.

### 3.2.1.1 Finite on-resistance of MOS switch

In reality, the MOS switch has finite resistance that is in series with the sampling capacitor  $C_S$ . Hence, the circuit has finite bandwidth with a time constant  $R_{on}C_S$  and an acquisition time is needed before the circuit can track the input.

The finite bandwidth also causes the circuits to track the input with a tracking error. The transfer function of the SH circuit during sampling time is equivalent to a linear filter with the time constant  $\tau = R_{on}C_S$ , i.e.

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + s\tau} \quad (3.1)$$

We can see,  $V_o/V_i=1$ , only when  $S=0$ . For other signal frequencies, the SH circuit will introduce a tracking error, but it doesn't affect the linearity of the SH. However, the  $R_{on}$  of the MOS switch increases nonlinearly with the input signal. Also  $C_j$  (junction capacitance of the MOSFET) decreases nonlinearly with the input signal. The tracking error due to the nonlinearity of the MOS switch contributes to the nonlinearity of the SH [Lin96].

### 3.2.1.2 Charge injection

An important error source of a MOS switch is charge injection [Wegmann87]. When the switch is on, some charge is present in the MOS channel. This is a result of forming a conducting channel under the MOS gate. The charge in the channel is on the order of  $C_{ox}WL(V_{gs} - V_t)$ . When the switch is turned off, charge flows to the source or the drain or is injected into the substrate and will create a small  $\Delta V = \Delta Q/C$  on the sampling capacitor, where  $\Delta Q$  is a function of input impedance, source impedance, clock falling edge, etc.

Therefore transition error occurs due to the channel injection when the MOS switch is turned off. The fixed component of the charge injection appears as a DC offset and hence can be easily calibrated out. The signal dependent component of the charge injection is more difficult to calibrate out. But using a fully differential approach and a clever clocking scheme the first order error can be eliminated if the matching is perfect.

The droop error comes from the leakage of the switch and can be neglected in high-speed CMOS designs since the leakage time is rather short.

### 3.2.1.3 Signal-dependent sampling

Besides all the errors mentioned above, there is a major problem with this simple scheme: signal-dependent sampling. It happens because the turn-off instant of a MOS switch depends on the signal at the source. It causes the signal-dependent distortion, which contributes to nonlinearity of the circuit. This is the reason a conventional S/H utilizes opamp-based switched capacitor technique.

### 3.2.2 Multiplying digital-to-analog converter

Figure 3.5 shows the schematic of our fully differential MDAC[Lewis92]. It consists of an opamp, six capacitors and 15 switches including a center sampling switch. Figure 3.6 shows the timing diagram of the clocks. The two main clocks,  $\Phi_1$  and  $\Phi_2$ , are nonoverlapping. To reduce the sample-to-hold transition error, two extra clocks,  $\Phi_{1-}$  and  $\Phi_{1+}$  are also used.

We can see more clearly the way this MDAC works in Figure 3.7.

1) When  $\Phi_1$ ,  $\Phi_{1-}$  and  $\Phi_{1+}$  are high, switches M1 ~ M9 are on, the opamp inputs are connected to each other and the common-mode voltage, at the same time, the opamp outputs are also reset to the common-mode voltage. The voltage on the “0.9C” sampling capacitors and “C” integrating capacitors tracks the input.

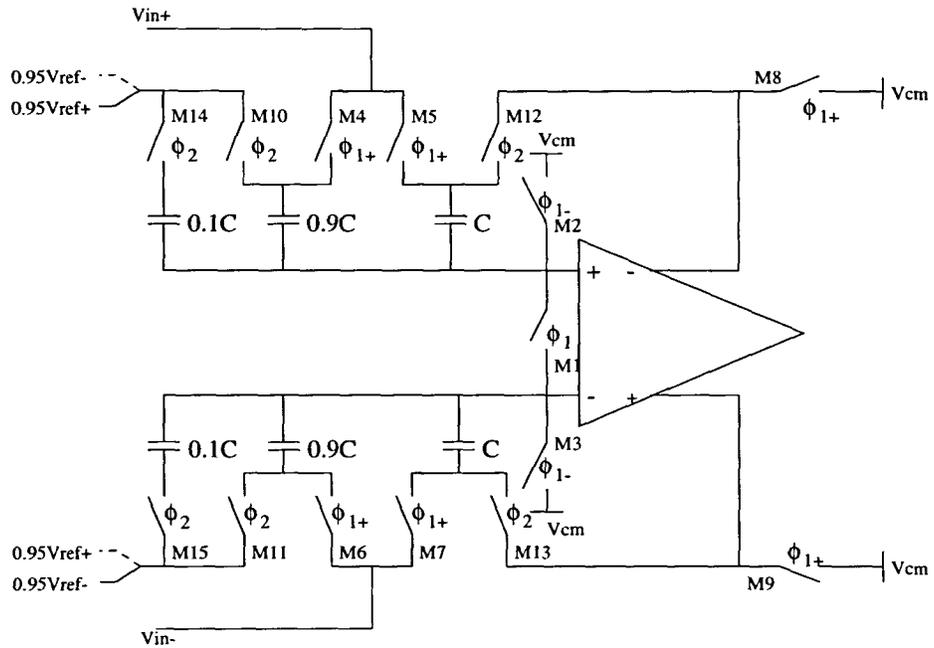


Figure 3.5 A fully differential multiplying DAC

2) When  $\Phi_{1-}$  goes low, the inputs of the opamp are released from the common-mode voltage but remain connected to each other through M1. M2 and M3 are chosen to be much smaller than M1 so that the charge injection error is small and decreases exponentially until M1 is turned off.

3) Then  $\Phi_1$  goes low and M1 is turned off. The signal is sampled on the sampling capacitors as well as the integrating capacitors. If the size of M1 is chosen to be

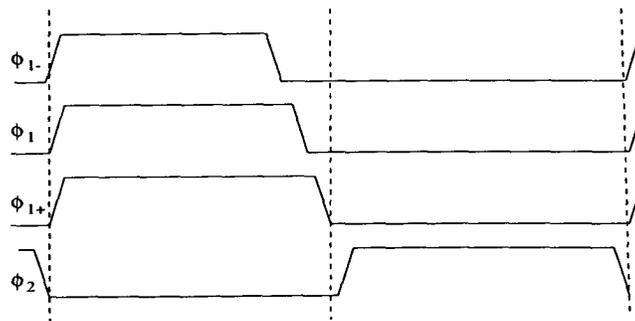


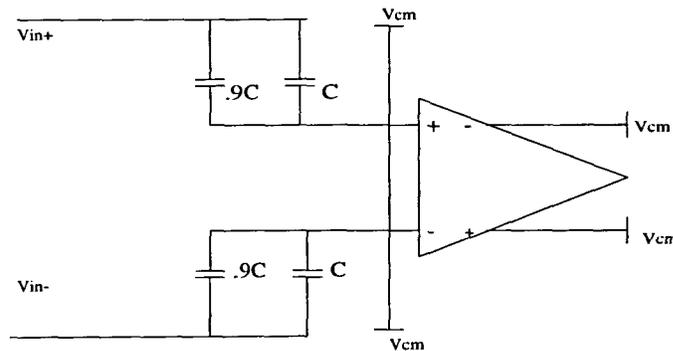
Figure 3.6 Timing Diagram

large enough, the charge injection from M1 is approximately distributed evenly onto the two input nodes and will not appear on the output since a differential configuration is used [Lin91].

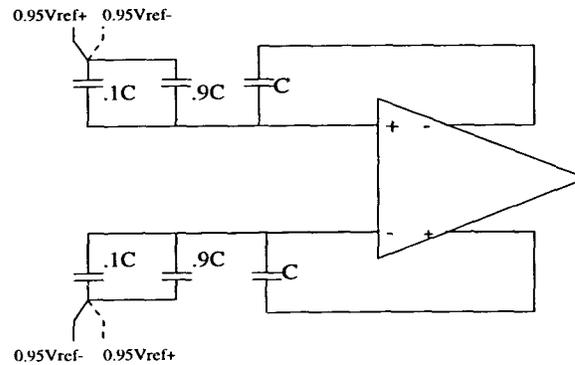
4) Then  $\Phi_{1+}$  goes low, and M4, M5, M6, M7, M8 and M9 are turned off. Since the charge on the bottom plates of the capacitors has no place to go, the charge injection from these switches does not affect the charge on the capacitors. Hence, it has no effect on the sampled signal. This is called bottom plate sampling. M4, M5, M6 and M7 are chosen to be large to reduce the effects of nonlinear resistance and impedance mismatch.

During  $\Phi_1$ , neglecting the opamp offset, the charge stored on the capacitors is

$$Q_1 = V_{in}(0.9C + C) = 1.9V_{in}C \quad (3.2)$$



(a) MDAC during sampling phase



(b) MDAC during amplifying phase

Figure 3.7 MDAC during different clock phases

During  $\Phi_2$  (Fig3.7b), the integrating capacitors are connected to the opamp outputs and the sampling capacitors in addition to the “0.1C” capacitors connected to the positive reference or the negative reference depending on the digital input which is the digital output of the previous stage.

$$Q_2 = V_{out}C \pm 0.95V_{ref}(0.9C + 0.1C) = V_{out}C \pm 0.95V_{ref}C \quad (3.3)$$

Since the charge is equal during two phase, the transfer function of the MDAC is given by:

$$V_{out} = 1.9V_{in} \pm 0.95V_{ref} \quad (3.4)$$

The resulting output consists of two parts: one arising from the feedforward of the integrating capacitors and another arising from the charge transfer between the sampling and integrating capacitors. Since only the second part is ratio dependent, the feedforward reduces the effect of capacitor mismatch on the interstage gain. This is important because the accuracy of the interstage gain of 2 determines the linearity of the ADC.

Besides the feedforward, there are two other motivations for sharing the integrating capacitors, which means the integrating capacitors are used as sampling capacitors during sample mode.

Firstly, the value of the sampling capacitors is determined by the value of  $\frac{KT}{C}$  noise that can be tolerated. For a sampling capacitor of 2pF,

$$\overline{dv^2} = \frac{KT}{C} = \frac{41.4 \times 10^{-22}}{2 \times 10^{-12}} = 20.7 \times 10^{-10} V^2 \quad (3.5)$$

which gives an equivalent voltage noise of 45uV per sample, corresponding to 0.11sb for 11-bit ADC with 1V peak input signal. By sharing the integrating capacitors, the size of sampling capacitor can be reduced about 50% which results in considerable die area saving.

Secondly, the speed of a pipelined ADC is always limited by the opamp settling time in the S/H “hold” phase. To optimize the speed, we want to maximize the loop transmission bandwidth which is determined by the following equation:

$$\omega_{lt} = F_b \times GBW \quad (3.6)$$

in which the feedback factor  $F_b$ , if ignoring the parasitics, is given by

$$F_b = \frac{C_F}{C_S + C_F} = \frac{1}{2} \quad (3.7)$$

Without sharing the integrating capacitor, the feedback factor in a conventional S/H is 1/3 since  $C_S = 2C_F$ . Therefore the speed is 50% higher compared to the conventional scheme.

### 3.2.3 Operational amplifier architecture

The MDAC discussed above includes an operational amplifier. This opamp, more accurately called operational transconductance amplifier, is a key block that limits the performance of the MDAC and furthermore, the performance of the ADC.

In high-speed high-resolution pipelined structure, the two most severe requirements of the opamp are the DC gain and settling time. To achieve 11-bit resolution, the DC gain of  $2^{12}$  is required. In general, a safety margin of 2x factor is taken into consideration; therefore the DC gain of the opamp,  $A$ , is usually required to be at least  $2^{13}$ . For a 50M application, assuming 50% duty cycle, the settling time is less than 10ns. Fast settling of the opamp requires a high unity-gain frequency. However, the realization of a CMOS operational amplifier that combines high DC gain with high unity-gain frequency has been a problem[Bult90].

The high gain requirement leads to multistage designs with long-channel devices biased at low current levels, whereas the high unity-gain frequency requirement calls for a single-stage design with short-channel devices biased at high current levels. Cascoding

is a well-known approach to enhance the DC gain of an amplifier without degrading the high-frequency behavior. However the enhancement is not enough for our application.

In this design, a gain-boosted fully differential folded-cascode amplifier is implemented. Based on the gain-boost principle, we were able to boost the DC-gain and achieve a satisfactory settling behavior as well.

The next section will discuss the details of the operational transconductance amplifier design.

### 3.2.3.1 Fully differential Folded-cascode opamp

In order to increase the open-loop gain, cascode techniques are often applied in opamp design. Although telescopic-cascode opamp has been used by many other designs for high-speed applications [Kim96][Lewis92][Bright98], its main disadvantage is its limited output swing. Its output swing will be less than the output swing of a folded-cascode architecture by one  $V_{dsat}$ , which is about several hundred millivolt. So we chose a folded-cascode architecture since large output swing is more desired in the low voltage (3.3V) design.

The basic idea of the folded-cascode opamp is to apply cascode transistors to the input differential pair but using transistors opposite in type from those used in the input stage. Figure 3.8 shows a fully differential folded-cascode amplifier. The differential-pair transistors M1 and M2 are n-channel transistors whereas the cascode transistors M5 and M6 are p-channel transistors. This arrangement of opposite-type transistors allows the output of the amplifier to be taken at the same bias-voltage level as the input signals, i.e. the output common-mode voltage can be set at the same level as the input common-mode voltage, which is convenient for pipelined architecture since the output signal of one stage would be the input for the next stage.

The small signal model of the opamp is shown in Figure 3.9.

The dominant pole of the system is due to the load capacitor and the second pole is

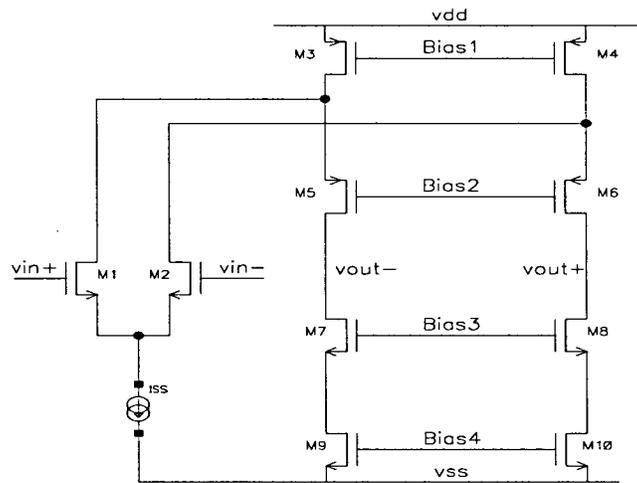


Figure 3.8 Schematic of a fully differential folded-cascode opamp

caused by the parasitic capacitors at the source of the cascode pair M5 and M6. The unity-gain frequency of the opamp is

$$GBW = \frac{g_{m1}}{C_L} \tag{3.8}$$

The DC gain is on the order of  $(g_m r_o)^2$  and given by

$$A_0 = - \frac{g_{m1}}{\frac{g_{d7}g_{d9}}{g_{m7}} + \frac{(g_{d3}+g_{d1})g_{d5}}{g_{m5}}} \tag{3.9}$$

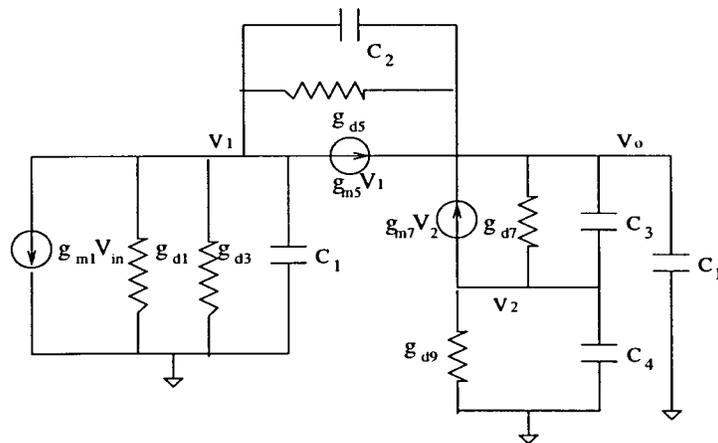


Figure 3.9 small-signal equivalent circuit for folded-cascode amplifier

The load of this opamp would be the sampling capacitors of the next stage including the shared integrating capacitor, and the gate capacitor of the comparator. The equivalent value of these capacitors is 3pF. With a capacitor load of 3pF, the AC simulation shows single-ended DC gain is 142, the unity-gain bandwidth is 725MHz and the phase margin is 59 degrees. However when we put the second stage as its load, the frequency responses are quite different from the above results. This is because in real applications, as shown in Figure 3.10 the output is connected with the sampling capacitors of the next stage through the serial switches.

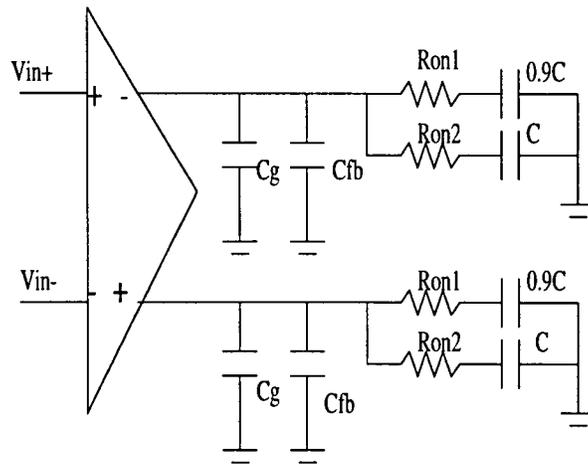


Figure 3.10 Load of opamp in pipelined application

The on-resistance of the sampling switches will introduce a zero into the system and therefore change the frequency behaviour of the opamp. The simulation is run again with the load same as shown in Figure 3.10, and the unity-gain bandwidth is dropped to 643MHz while the phase margin is improved to 75 degree as shown in Figure 3.11 and 3.12.

The common-mode feedback circuit which is needed for the fully differential opamp is not shown in Figure 3.8. And it will be covered in section 3.2.3.5.

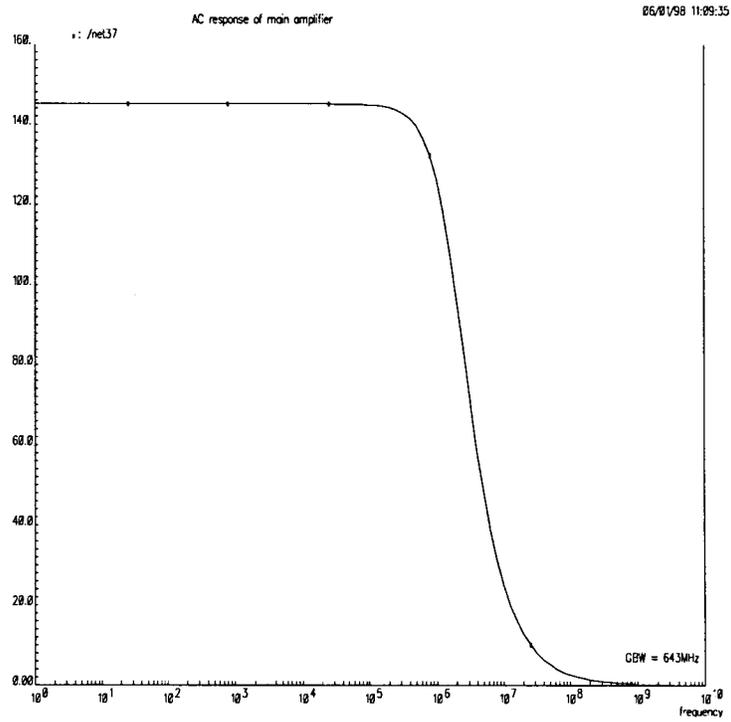


Figure 3.11 AC response of folded-cascode amplifier: magnitude

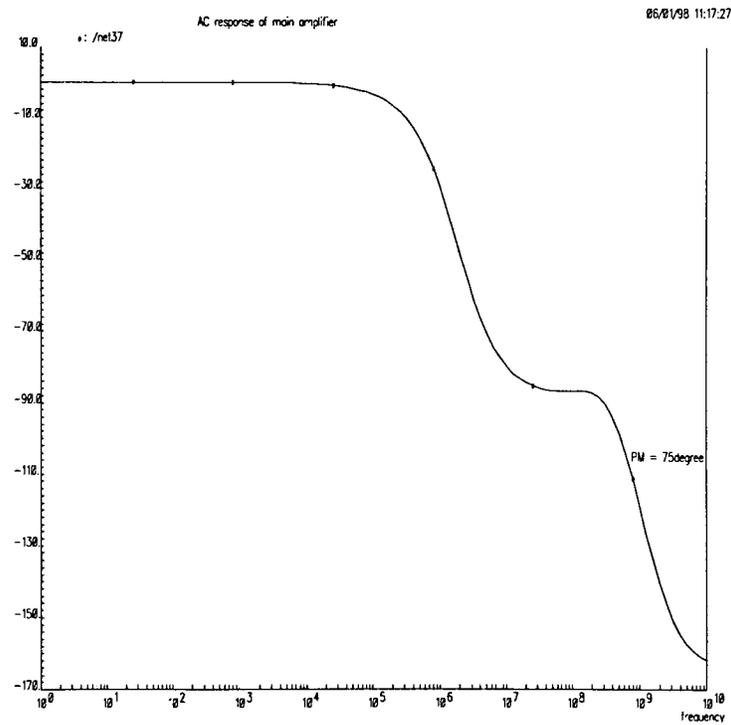


Figure 3.12 AC response of folded-cascode amplifier: phase

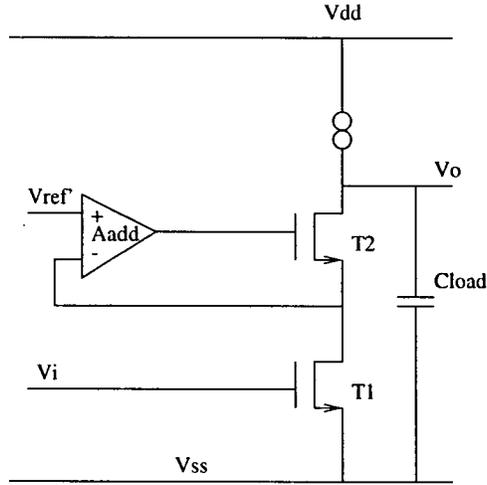


Figure 3.13 Cascode gain stage with gain enhancement

### 3.2.3.2 Principle of gain-boosting

The gain-boost technique [Bult90] is based on increasing the cascoding effect of T2 by adding an additional gain stage as shown in Figure 3.13. This stage reduces the feedback from the output to the drain of the input transistor. Thus, the output impedance of the circuit is increased by the gain of the additional gain stage,  $A_{add}$ :

$$R_{out} = (g_{m2}r_{o2}(A_{add} + 1) + 1)r_{o1} + r_{o2} \quad (3.10)$$

The DC-gain can be increased by several orders of magnitude:

$$A_{o,tot} = g_{m1}r_{o1}(g_{m2}r_{o2}(A_{add} + 1) + 1) \quad (3.11)$$

In Figure 3.14, a gain plot is shown for the original cascoded gain stage ( $A_{orig}$ ), the additional gain stage ( $A_{add}$ ), and the improved cascoded gain stage of Fig3.13 ( $A_{tot}$ ). From equation 3.10, we know at dc, the gain enhancement  $A_{tot}/A_{orig}$  equals approximately  $[1+A_{add}(0)]$ . For  $\omega > \omega_1$  (the 3-dB frequency of the improved stage), the output impedance of the improved stage is mainly due to  $C_L$  which results in a first-order roll-off of  $A_{tot}(\omega)$ . Furthermore it implies that  $A_{add}(\omega)$  may have a first-order roll-off for  $\omega > \omega_2$  (the 3-dB frequency of the additional stage) as long as  $\omega_2 > \omega_1$ . This is equivalent to

the condition that the unity-gain frequency ( $\omega_4$ ) of the additional gain stage has to be larger than the 3-dB frequency ( $\omega_3$ ) of the original stage, but it can be much lower than the unity-gain frequency  $\omega_5$  of the original stage. The improved gain stage has the same unity-gain frequency as the original stage. Hence the additional stage needs not be fast with respect to the unity-gain frequency of the original design.

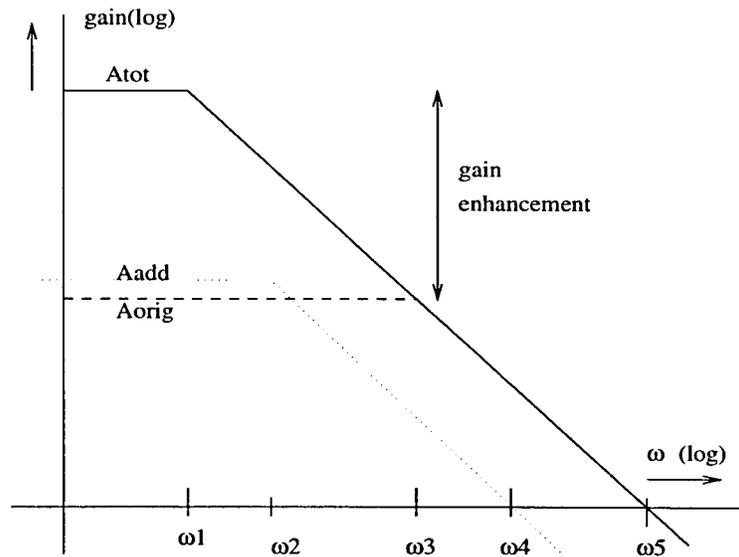


Figure 3.14 Bode plots of the original, additional and improved gain stage

In fact, due to stability reasons, the unity-gain frequency of the additional stage needs to be set at lower than the second-pole frequency of the main amplifier  $\omega_6$ . A safe range for the location of the unity-gain frequency  $\omega_4$  of the additional stage is given by

$$\omega_3 < \omega_4 < \omega_6 \quad (3.12)$$

### 3.2.3.3 Boosting amplifier design

For the folded-cascode main amplifier, we need two types of additional stage: one for boosting the p-channel transistors M5 and M6, another for boosting the n-channel transistors M7 and M8. Since boosting amplifiers will introduce more poles and zeros to the improved opamp, we were targeting a simple way to realize them.

Figure 3.15 shows the PMOS-boasting amplifiers [Kim96].

Devices M0 and M1 are used as a dc level shifter, and so are M2 and M3. A NMOS differential stage, composed of devices M4, M5, M6, M7 and M8, is used for gain enhancement. Since the boosting amplifiers need not to be fast, the power and the area could be much smaller than the original amplifier. The DC gain of this amplifier is in the order of  $g_m r_o$ .

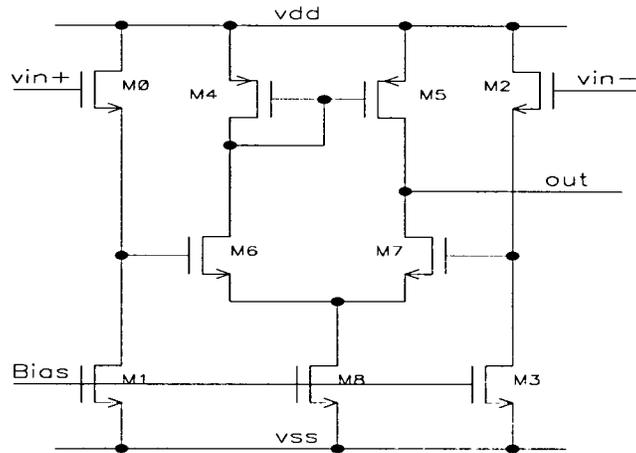


Figure 3.15 PMOS boosting amplifier

The PMOS-boasting amplifier has a DC gain of 44. This amplifier is designed with a unity-gain bandwidth of 500MHz as well as 45 degree of phase margin. However due to the compensation capacitance added at its output (it will be covered in next section), the GBW decreases significantly to 258MHz while the phase margin increases to 65 degree as shown in Figure 3.16 and 3.17.

Figure 3.18 shows the schematic of NMOS-boasting amplifier. It would be more natural to choose the complementary type of devices as used in PMOS-boasting amplifier. However, PMOS in this submicron process is much weaker than NMOS ( $\mu_n/\mu_p > 3$ ). Therefore, we are still using NMOS differential stage due to its relatively higher gain. The price paid is one more bias voltage.

The frequency behavior of NMOS-boasting amplifier is not so important as the

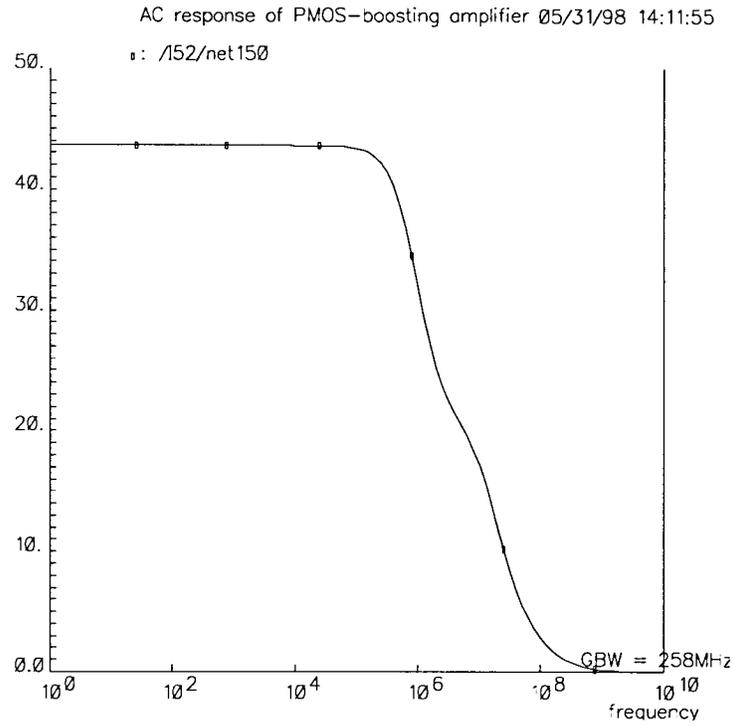


Figure 3.16 AC response of PMOS boosting amplifier: magnitude

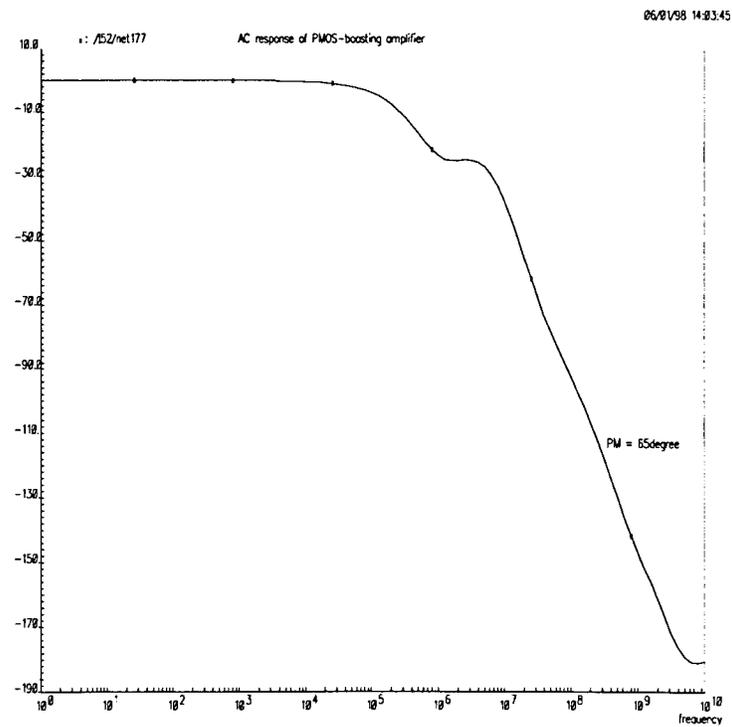


Figure 3.17 AC response of PMOS boosting amplifier: phase



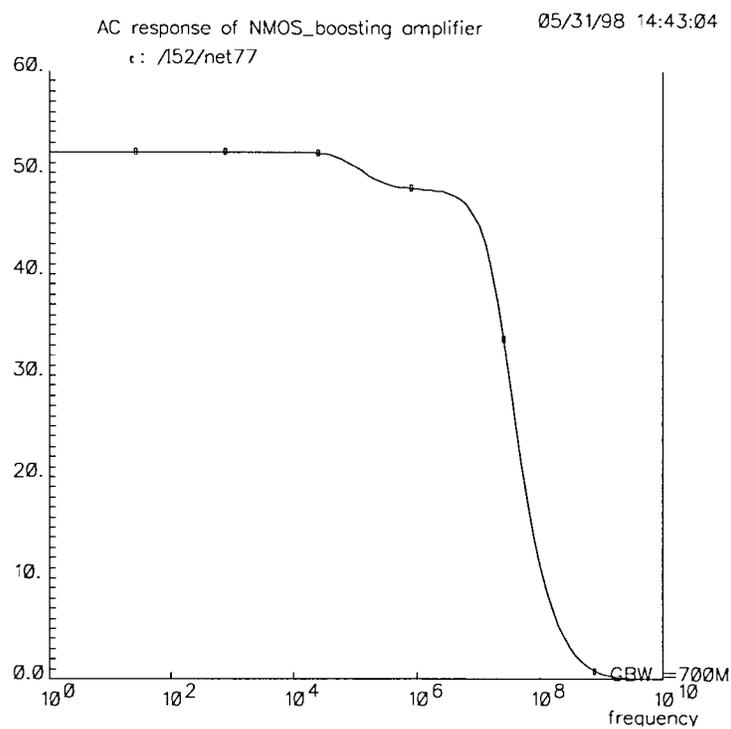


Figure 3.19 AC response of NMOS boosting amplifier: magnitude

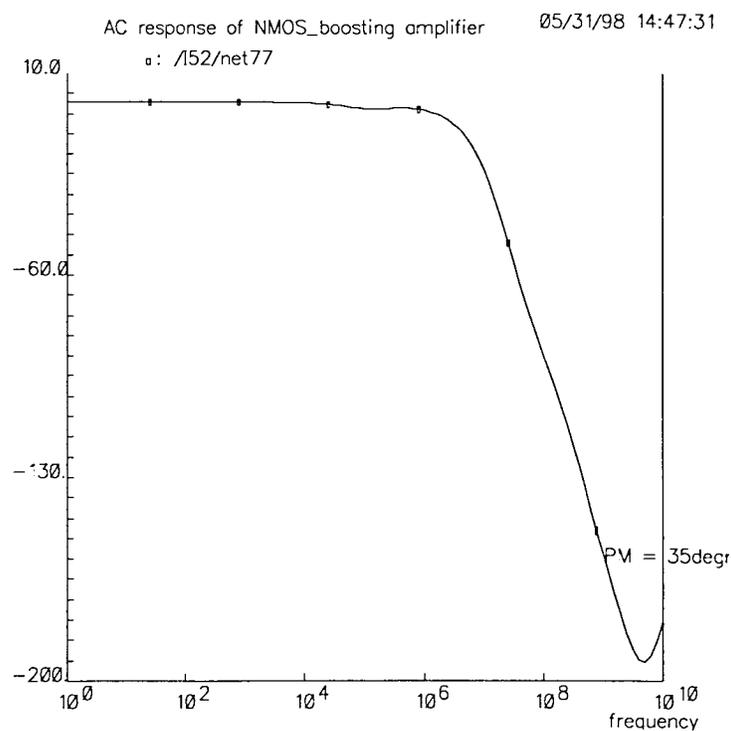


Figure 3.20 AC response of NMOS boosting amplifier: magnitude

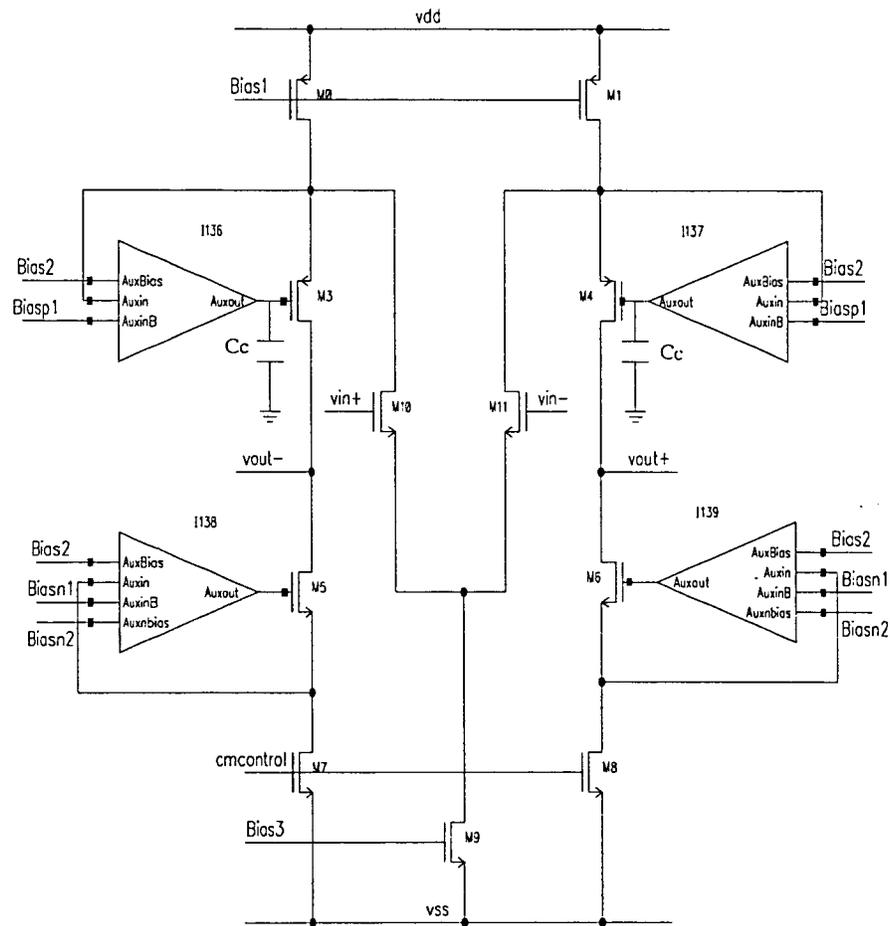


Figure 3.21 A gain-boostered fully differential folded-cascode amplifier

When the opamp is slewing, the maximum current available for the slew rate is limited by the bias currents of transistors M7 or M8 in Figure 3.21. Even if the common-mode feedback circuit is fast, the slew rate of a fully differential opamp is seldom to the degree of a single-ended output opamp. For this reason, fully differential folded-cascode opamps are usually designed with the bias currents in the output stage equal to the bias currents in the input transistor pair [Johns97]. For high-speed applications, this current is fairly large. In our design, the currents in M7 and M9 are biased at 2mA.

Neglecting second-order effects, the equation describing the behavior of a MOS tran-

istor in saturation region is

$$I_D = \frac{\mu C_{ox} W}{2L} (V_{GS} - V_T)^2 \quad (3.13)$$

and  $W/L$  can be calculated by

$$\frac{W}{L} = \frac{2I_D}{\mu C_{ox} (V_{GS} - V_T)^2} \quad (3.14)$$

The currents of the opamp are

$$I_7 = I_5 = I_3 = I_8 = I_6 = I_4 = 2mA$$

$$I_9 = I_0 = I_1 = 4mA$$

$$I_{10} = I_{11} = 2mA$$

The MOS transistors in the opamp are usually biased at a low excess voltage  $V_{GS} - V_T$ .

The desired excess voltages for the transistors are following:

$$V_{10} = V_{11} = 150mV$$

$$V_7 = V_5 = V_8 = V_6 = 200mV$$

$$V_9 = V_0 = V_1 = 400mV$$

$$V_3 = V_4 = 300mV$$

The input pair has a minimum excess voltage for maximizing the  $g_m$  and furthermore the unity-gain frequency of the opamp. Since transistors M9, M0 and M1, the currents are 4mA. In order to reduce the transistor size, the excess voltage is chosen to be 400mV. For the PMOS cascode transistor pair, the excess voltage is chosen to be 300mV for increasing the  $g_m$  with a moderate size since the PMOS is rather weak in this process.

Typical value for  $\frac{1}{2}\mu C_{ox}$  is  $112.7\mu A/V^2$  for NMOS and  $24.8\mu A/V^2$  for PMOS. Knowing the currents, the excess voltage and the above parameters, we can estimate the initial

sizes of the transistors of the main opamp.

$$\begin{aligned}
 M9 : \frac{W}{L} &= \frac{4 \times 10^{-3}}{112 \times 10^{-6} \times (0.4)^2} = 223 \\
 M10, M11 : \frac{W}{L} &= \frac{2 \times 10^{-3}}{112 \times 10^{-6} \times (0.15)^2} = 773 \\
 M5, M6, M7, M8 : \frac{W}{L} &= \frac{2 \times 10^{-3}}{112 \times 10^{-6} \times (0.2)^2} = 446 \\
 M0, M1 : \frac{W}{L} &= \frac{4 \times 10^{-3}}{24.8 \times 10^{-6} \times (0.4)^2} = 1008 \\
 M3, M4 : \frac{W}{L} &= \frac{4 \times 10^{-3}}{24.8 \times 10^{-6} \times (0.3)^2} = 896
 \end{aligned}$$

However in this digital  $0.35\mu\text{m}$  process, the channel length is short, thus the higher order effects are considerable. The final transistor sizes by simulation in level39 model is shown in the appendix.

The gain-boosted amplifier can achieve a gain proportional to  $(g_m r_o)^3$ . Figure 3.22 and 3.23 show the AC analysis results for the gain-boosted folded-cascode amplifier. Single-ended DC gain is 6128, so the differential gain is more than 12K i.e. 81dB. The phase margin is 59 degree and unity-gain bandwidth is 545MHz with  $C_c$  equal to 300fF.

### 3.2.3.5 Common-mode feedback circuit

One drawback of using fully differential opamps is that a common-mode feedback circuit(CMFB) must be added. This extra circuitry is needed to establish the common-mode output voltage. There are two typical approaches designing CMFB circuits; a continuous-time approach and a switched-capacitor approach. Because the opamp is used in a switched-capacitor circuit, we use the latter approach because switched-capacitor CMFB circuits are generally preferred over their continuous-time counterparts since they allow a larger output swing[Johns97]. The schematic of a switched-capacitor common-mode feedback circuit is shown in Figure 3.24.

The two capacitors are of equal size and should be included in the load of the opamp. During the sampling phase, the pair of capacitors are precharged to the proper value

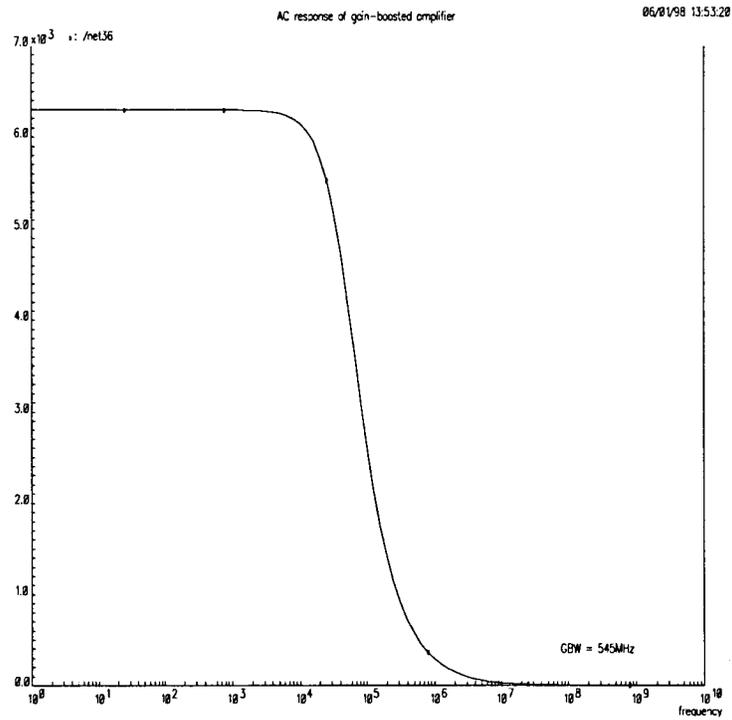


Figure 3.22 AC response of gain-booster folded-cascode amplifier: magnitude

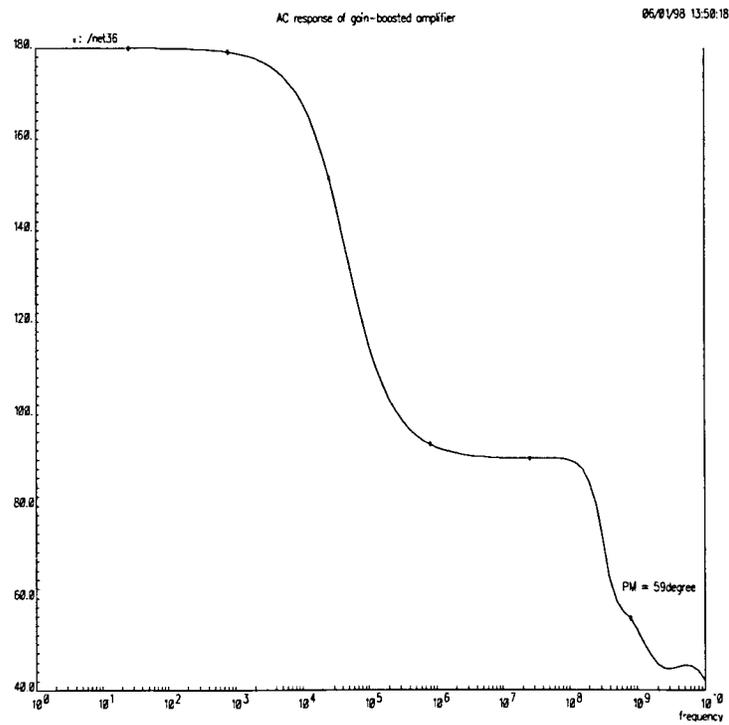


Figure 3.23 AC response of gain-booster folded-cascode amplifier: phase

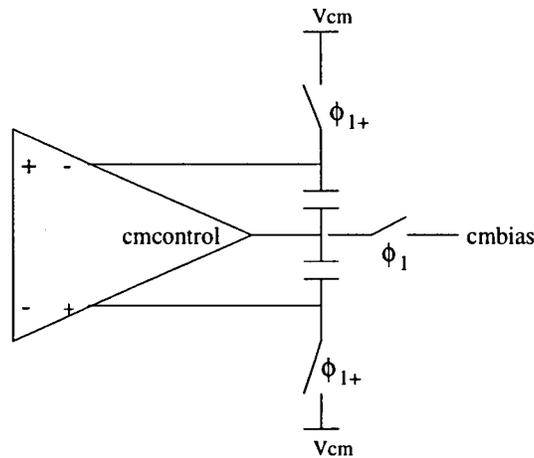


Figure 3.24 Common-mode feedback circuit

used in amplifying mode. During the hold phase, they are connected in a common mode feedback loop, creating the gate voltage of devices M7 and M8, and controlling the current source of the opamp.

Using excessively large capacitance overloads the opamp during amplifying phase, while reducing the capacitors too much causes common-mode offset voltage due to charge injection of the switches. We used a value of 300fF. The “cmbias” voltage is designed to be equal to the difference between the desired common-mode voltage and the desired control voltage used for the opamp current sources.

The “cmbias” is generated by a diode-connected transistor chain as shown in Figure 3.25. The generated voltage is -750mV when simulating with Level 39 nominal model. However when simulating using Level 39 slow model, the desired “cmbias” voltage changed to -684.9mv and the generated voltage is not close enough. Thus in addition to the transistor chain, this “cmbias” node can be also accessed by an off-chip voltage source which can be adjustable to track the process variation.

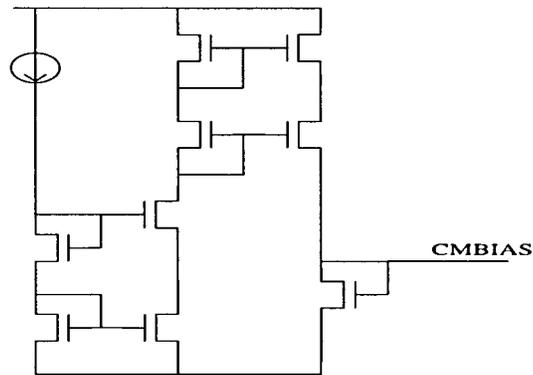


Figure 3.25 cmbias voltage generator

### 3.2.3.6 Bias circuit

To finish the discussion of the design of the opamp, Figure 3.26 shows the schematic of the bias circuit. This circuit uses a current source generated from a master current mirror as shown in Figure 3.27 to create six bias voltages including those needed by the boosting amplifiers.

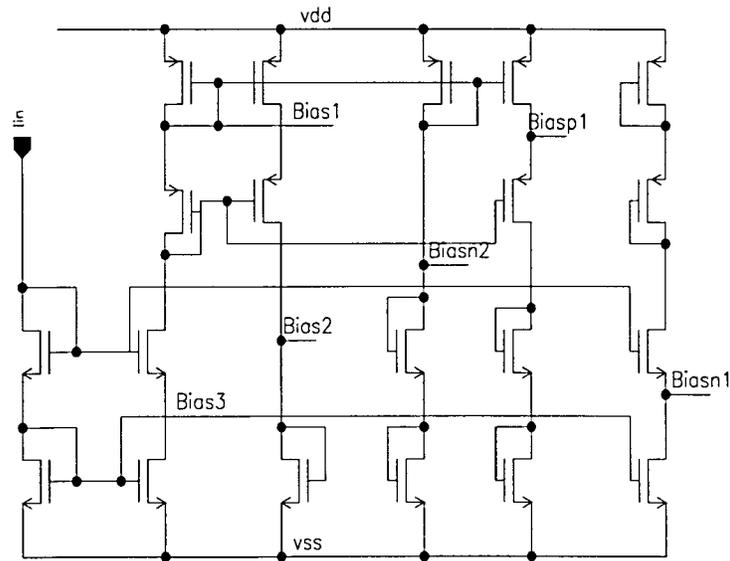


Figure 3.26 Bias circuit

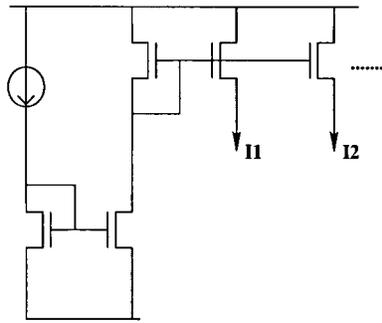


Figure 3.27 Master current mirror

### 3.2.4 Simulation results of MDAC

Now we are ready to present the simulation results of the multiplying digital-to-analog converter. Figure 3.28 shows the transient response of the MDAC. The square waveform is the hold clock signal. The MDAC is in amplify mode when it is high. The positive and negative output waveform are both shown in the figure as well as the differential output. With a differential input of 1.8V, we have the differential output of 1.70954V within 9ns, which means the MDAC has achieved 11-bit accuracy within 9ns.

Figure 3.29 is the block diagram of one cell which shows the differential connection between MDAC and the comparator. Since the operational transconductance amplifier is an inverting amplifier, the output needs to be switched when the MDAC is connected with the comparator.

## 3.3 Comparator Design And Simulation Result

In the final section, the comparator schematic and simulation results are presented. The comparator is designed by Ms. Hui Liu.

Figure 3.29 shows the schematic of a comparator. It consists of an OTA and two inverter stages and a D-latch. The worst case minimum resolvable signal is 4.3mv and the simulation result is shown in the Figure 3.30. The comparator is strobed when  $\Phi_2$

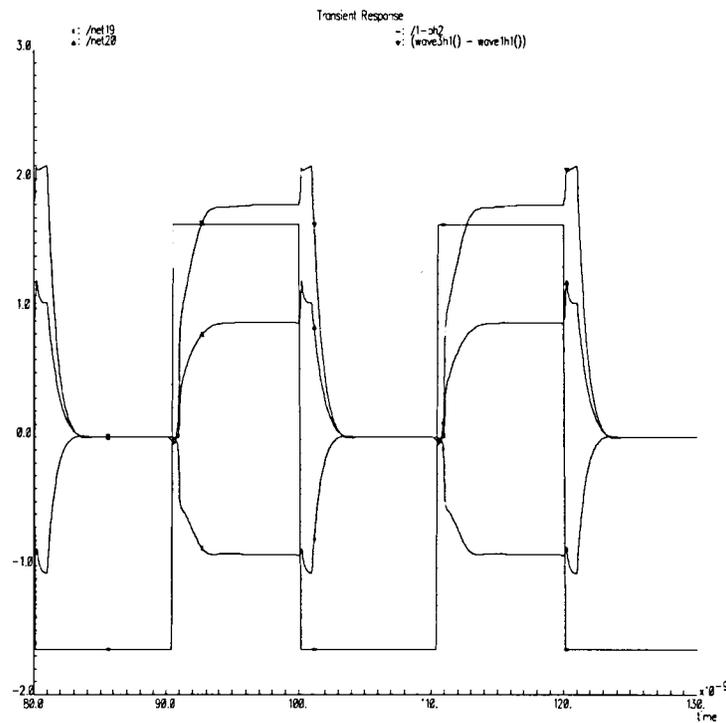


Figure 3.28 Transient analysis of the MDAC

goes low as shown in the timing diagram Figure 3.1.

### 3.4 Conclusion

In this chapter, the timing for the pipelined ADC is first discussed. The multiplying DAC design especially the opamp design is presented after an analysis of the errors

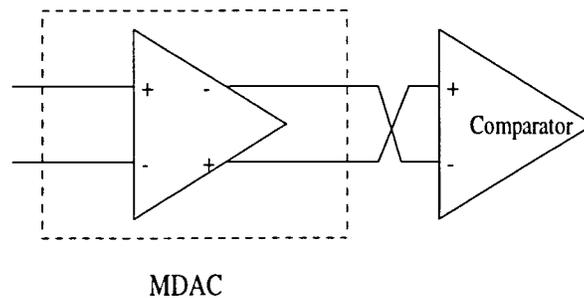


Figure 3.29 Differential connection between the MDAC and comparator

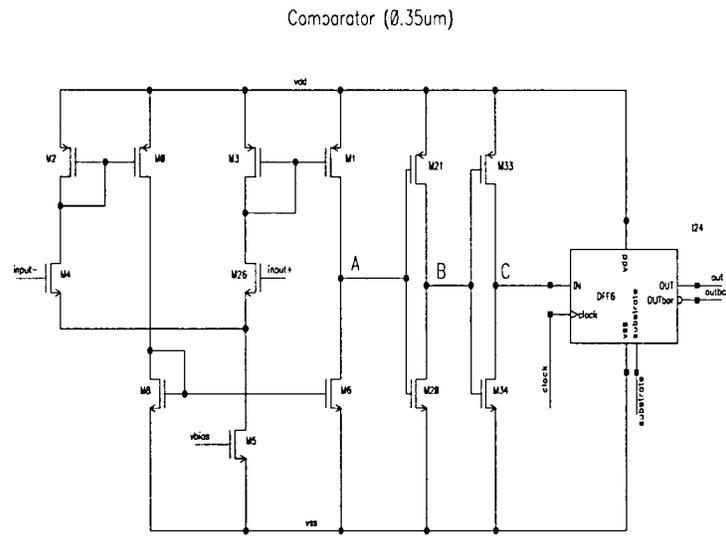


Figure 3.30 Schematic of the comparator

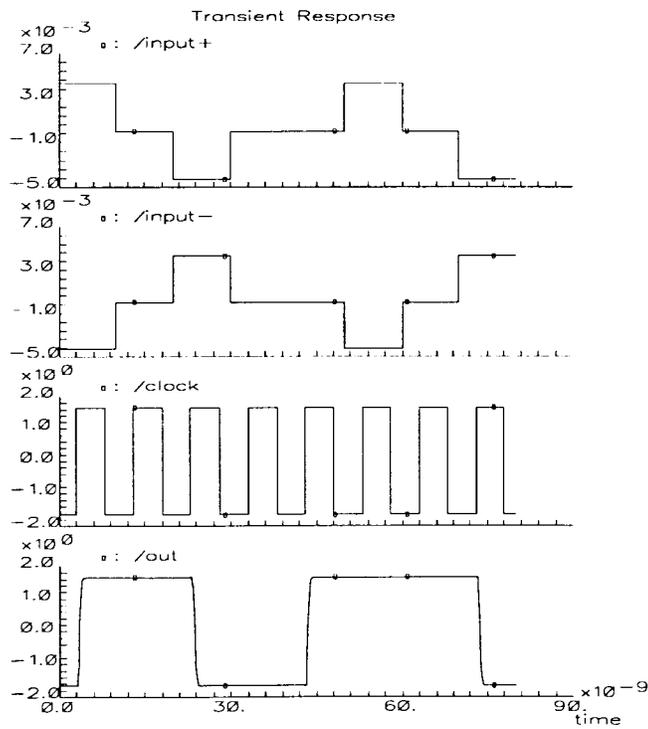


Figure 3.31 Transient analysis of the comparator

sources in sample-and-hold circuits. The comparator design was also described. Off-chip digital self-calibration will be performed for the convenience of testing the calibration algorithm. For the second fabrication pass, on-chip digital calibration logic will be implemented. As the conclusion of the design of the pipeline stage, the following tables list the overall specification.

Table 3.2 Gain-booster amplifier specification

DC gain	81dB
Unity-gain bandwidth	545MHz
Phase margin	59 deg
Slew rate	0.9V/ns

Table 3.3 MDAC specification

Settling time	$\leq 9\text{ns}$
Resolution	11-bit
Dynamic range	$\pm 0.9\text{V}$
Power dissipation	33mW

Table 3.4 Comparator specification

Min resolvable signal	4.3mV
DC gain	80dB
Power dissipation	0.9mW

## 4 SYSTEM SIMULATION RESULTS AND LAYOUT

In the previous chapters, we discussed the architecture of a 12b/50M ADC, especially the design of the multiplying DAC(MDAC). We also included the simulation results for MDAC as well as the comparator in chapter 4. In this chapter, we will present the SPICE simulation results of the system and discuss the layout design of the system. As mentioned in the previous chapter, the digital self-calibration is performed off-chip. Thus the layout of the digital calibration logic circuit is not covered here. The digitally self-calibrated ADC has two mode of operation: normal conversion mode and digital calibration mode. The configuration of the ADC for calibration will be covered in the last section of this chapter.

### 4.1 System Simulation Results

Before we begin the top level simulation with our non-binary gain stages, we simulated the system with the gain of all stages set to 2 for function verifications, since the digital output of a binary system is easier to interpret.

#### 4.1.1 System simulation results with gain of 2 MDAC

Figure 4.1 shows the block diagram of the top level binary radix simulation.

For a bipolar radix 2 pipelined ADC, missing codes and missing decision levels are most likely to happen near the major transition point. Hence we did the system simulation at the major transition point where the input signal is “0”. With a “1” digital

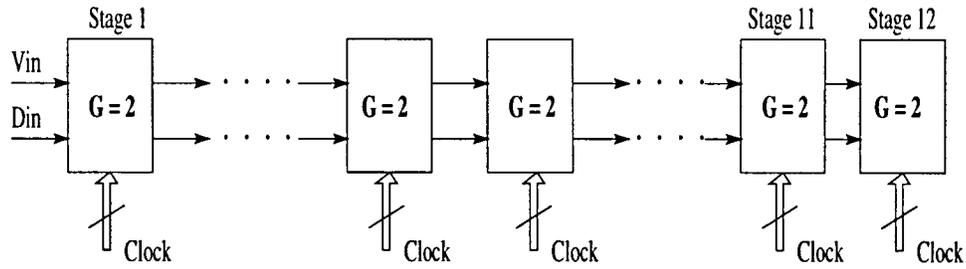


Figure 4.1 Top level block diagram with the interstage gain of 2

input, The waveform of digital outputs of 11 stages is shown in Figure 4.2, which shows the correct output “0000000000”. We also tested the other case, in which the digital input is “0” and the analog input is still “0”. And we had the right digital output code which was “1111111111”. The nets from the top to bottom in Figure 4.2 correspond to the digital outputs of all MX2 stages from stage 1 ~ 11.

#### 4.1.2 System simulation result with gain of 1.9 MDAC

This time, the gain of the multiplying DAC is switched from 2 to 1.9. The SPICE simulation results is shown in Figure 4.3. The digital input of the system was “1”, and the analog input was also zero, we had the digital output of “000010101010”. To verify the results, let us compare the measured results to the calculated results.

The measured digital outputs are no longer same as the calculated digital outputs starting from the 11th stage. The reason can be explained in Figure 4.4.

Table 4.1 Calculation and Measurement Results

Stage No.	$V_{out_{cal}}$	$D_{cal}$	$V_{out_{meas}}$	$D_{meas}$
Stage 1	$0 \times 1.9 - 0.855 \times 2 = -1.71$	0	-1.7095	0
Stage 2	$-1.71 \times 1.9 + 0.855 \times 2 = -1.539$	0	-1.5378	0
Stage 3	$-1.539 \times 1.9 + 0.855 \times 2 = -1.2141$	0	-1.2114	0
.	.	.	.	.
Stage 10	$0.4119 \times 1.9 - 0.855 \times 2 = -0.9139$	0	-0.51	0
Stage 11	$-0.9139 \times 1.9 + 0.855 \times 2 = -0.026$	0	0.75	1
Stage 12	$-0.026 \times 1.9 + 0.855 \times 2 = 1.6608$	1	-0.28	0

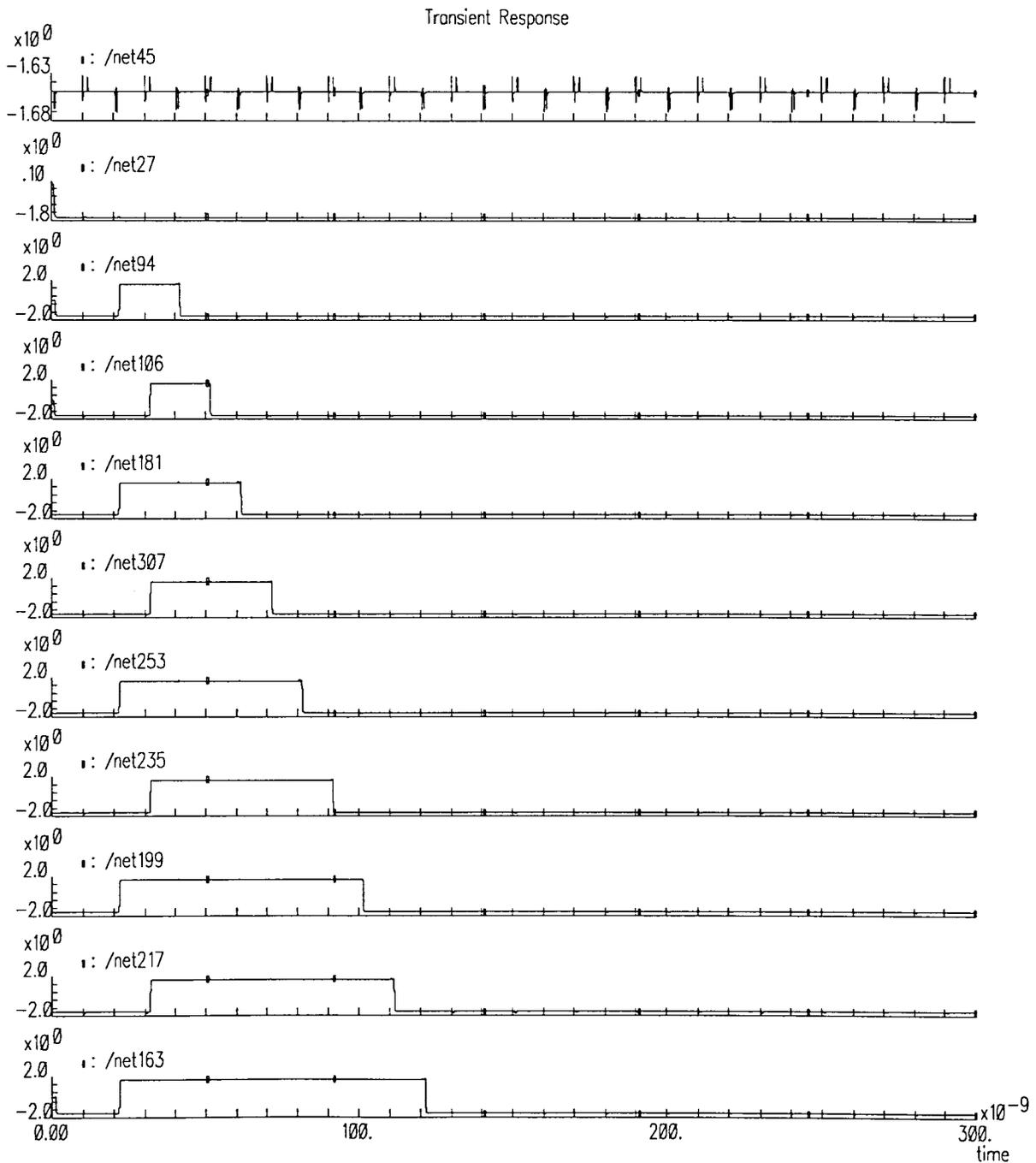


Figure 4.2 Top level simulation results with the interstage gain of 2

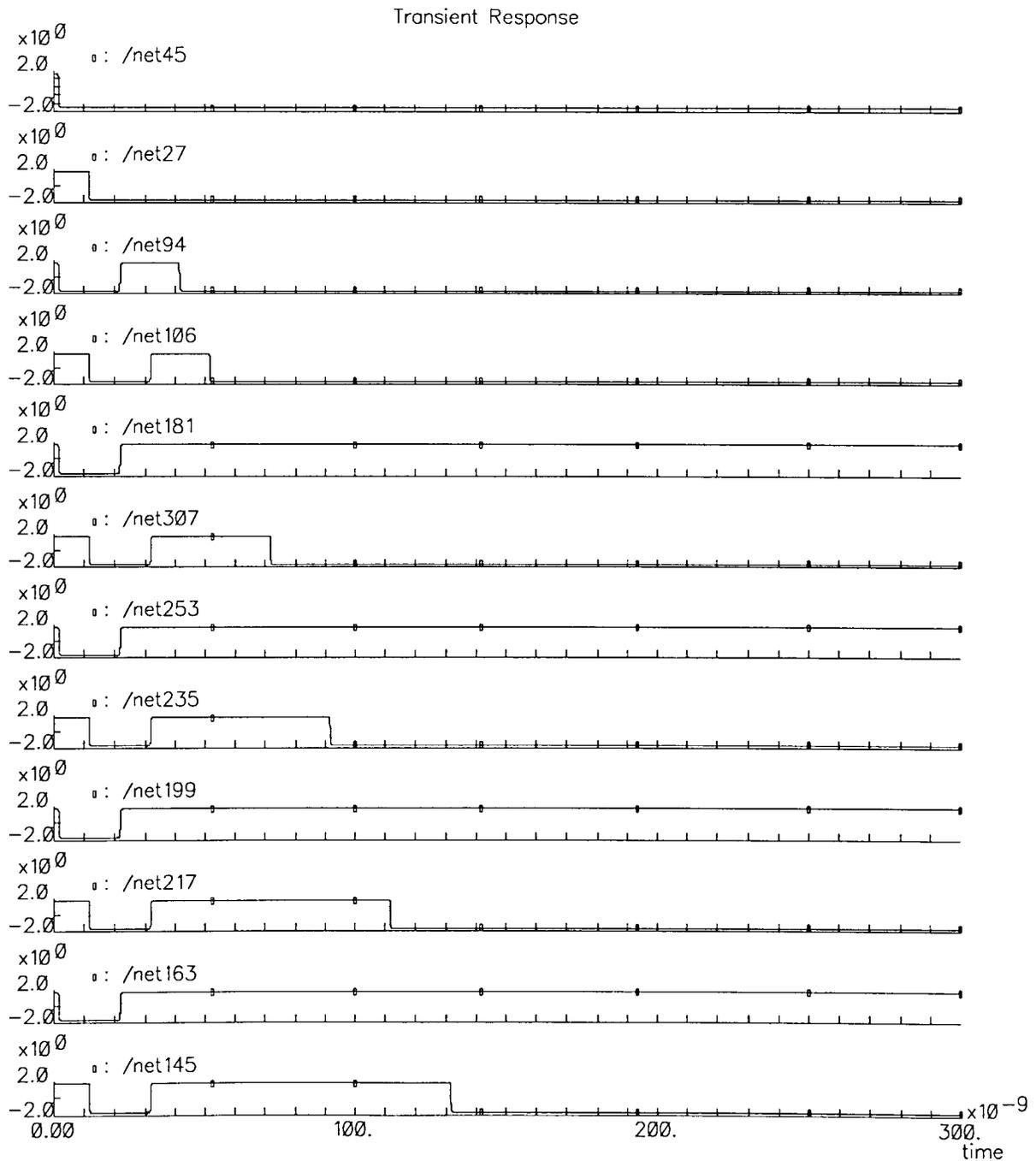


Figure 4.3 Top level simulation with 1.9X MDAC

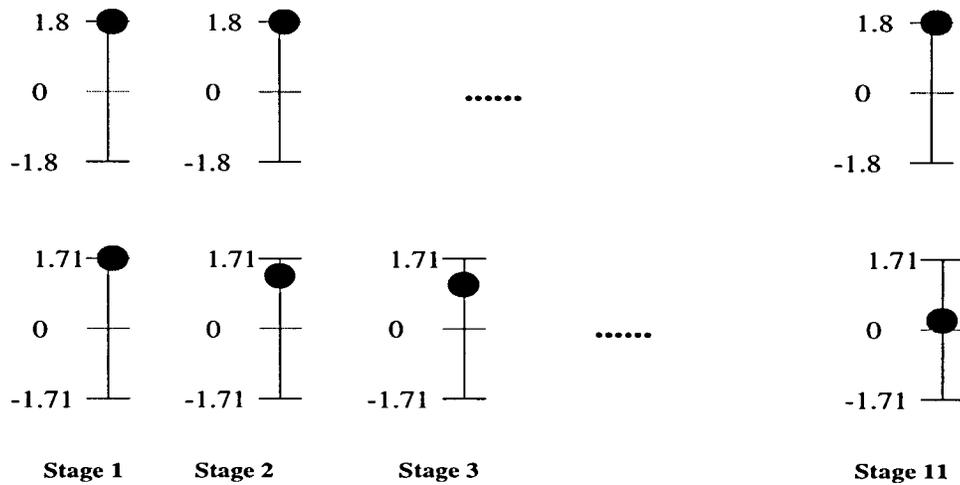


Figure 4.4 Reference scaling for gain of 2 and 1.9

When the interstage gain is set to 2, an input of  $V_{ref}$  of the first stage can be kept at full reference scale going down the stages. On the other hand, when the interstage is less than 2, the input  $V_{ref}$  would be scaled down. After some stages, 11 stages in our case, the calculated value without any error would be 0.026V, and it would be close to the threshold of the comparator. The comparator can easily make a wrong decision.

## 4.2 Layout Considerations

For such a large mixed-signal system as a 12b/50M pipelined ADC, we will need a hierarchical layout scheme to design effectively. Fortunately an advantage of the pipeline ADC is that it is easy to realize hierarchically. Once the layout of a single stage is completed, the layout of the whole pipeline can proceed rapidly. The floorplan of the pipelined ADC is shown in Figure 4.5.

The resolution targeted by our design requires careful layout. The effect of digital circuit noise has been one of the major sources of degradation in performance in the ADC. The analog signals are kept far away from the digital area in order to avoid digital noise coupling. Therefore all the clock buffers and input clock line are located in either

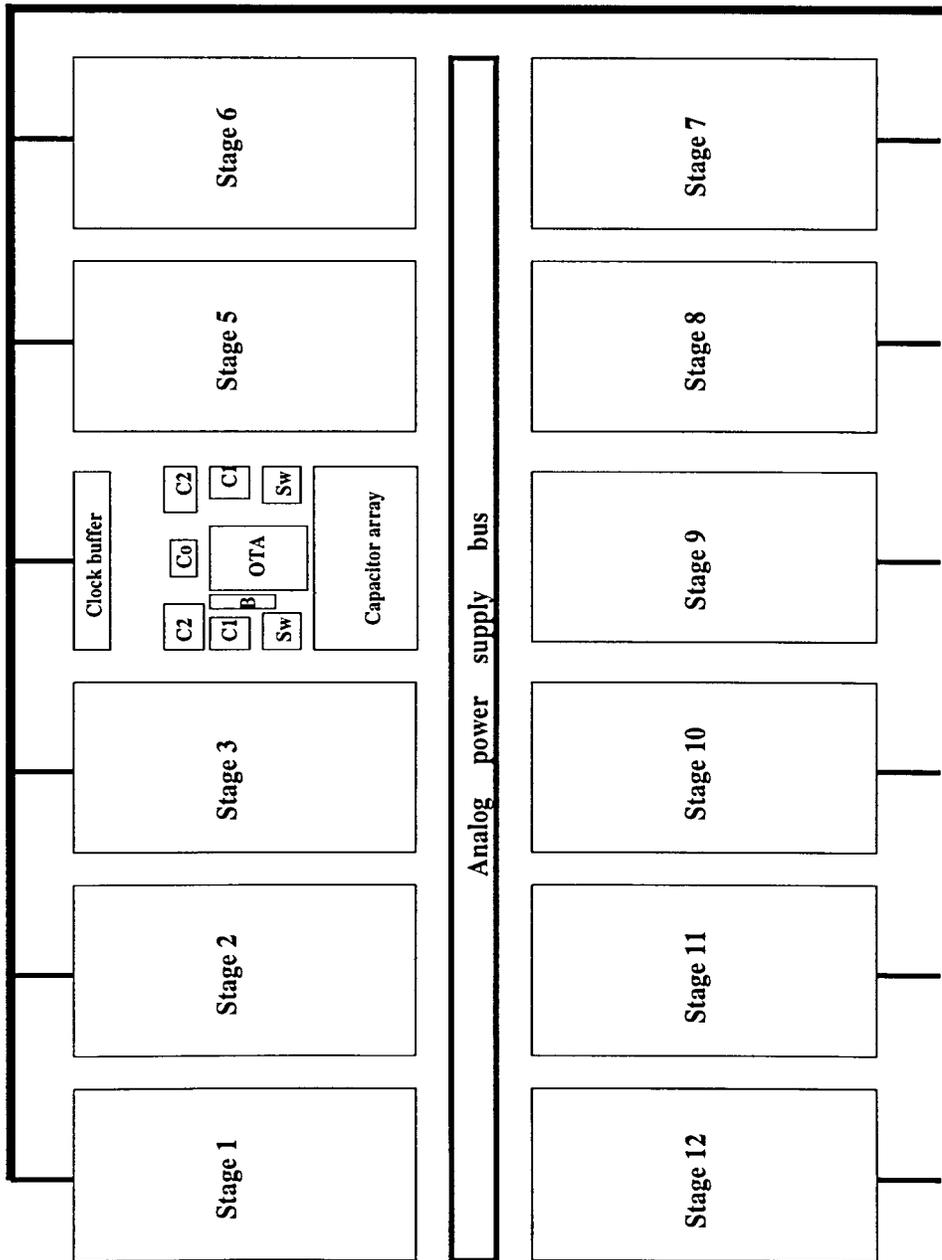


Figure 4.5 Floorplan of the pipelined ADC

top or bottom part of the chip.

In Figure 4.5, 12 stages of pipelined ADC are shown. The 4th stage is shown in more detail although all the stages are identical.

Now we are ready to discuss the details of the layout of subblocks.

#### 4.2.1 Operational transconductance amplifier layout

Since the operational transconductance amplifier (OTA) is the key and sensitive block, attention must be paid to its layout. It is a fully differential circuit. Therefore, symmetry of the layout must be attained. In order to reduce offset, the input pair is interdigitized. The same technique applies to the sensitive transistor pairs in order to reduce mismatch. The amplifier has its own biasing circuitry to make the wiring simpler in the overall layout.

#### 4.2.2 Capacitor layout

The capacitor layout is finished by Anil Tammineedi.

In  $0.35\mu\text{m}$  CMOS process, we do not have the option of standard linear capacitor. As shown in Figure 4.6, We implemented the capacitor by metal 2-3-4 sandwich because of its better voltage coefficient. Metal1 is not used to reduce parastic to substrate. Metal3 will be the top plate of the capacitor.

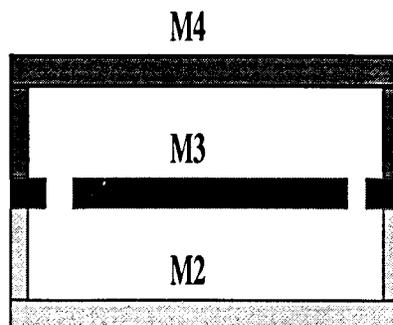


Figure 4.6 Metal-sandwich as a capacitor

In order to reduce gain error without trimming, we need to minimize the mismatch between the capacitors. Figure 4.7 shows the common-centroid capacitor arrays employed in the design.

In our design, the value for the feedback capacitor is 1pF. The sampling capacitor is composed by 0.1pF and 0.9pF. In Figure 4.7, “1” denote the 0.1pF, “9” for the 0.9pF and “10” for the 1pF. “D” refers to dummy capacitor. The top plates of the capacitors are connected with the input nodes of the OTA since the top plate has less parastic capacitance.

10	9	10	9	10
D	10	9	10	D
9	9	1	9	9
D	10	9	10	D
10	9	10	D	10

Figure 4.7 Common-centroid capacitor array

### 4.2.3 Layout of one stage

In the floorplan of the whole pipelined ADC, we showed the detailed arrangement of one stage. Sw is the switch circuit and C0 is the comparator. C1 is the 300fF capacitor in common-mode feedback circuit while C2 is the compensation capacitor which is needed by the OTA. Symmetry is still the goal of the layout of one cell. The layout of one stage is shown in Figure 4.8. and we can see the symmetry is achieved.

Finally the layout of the whole pipeline is shown in Figure 4.9.

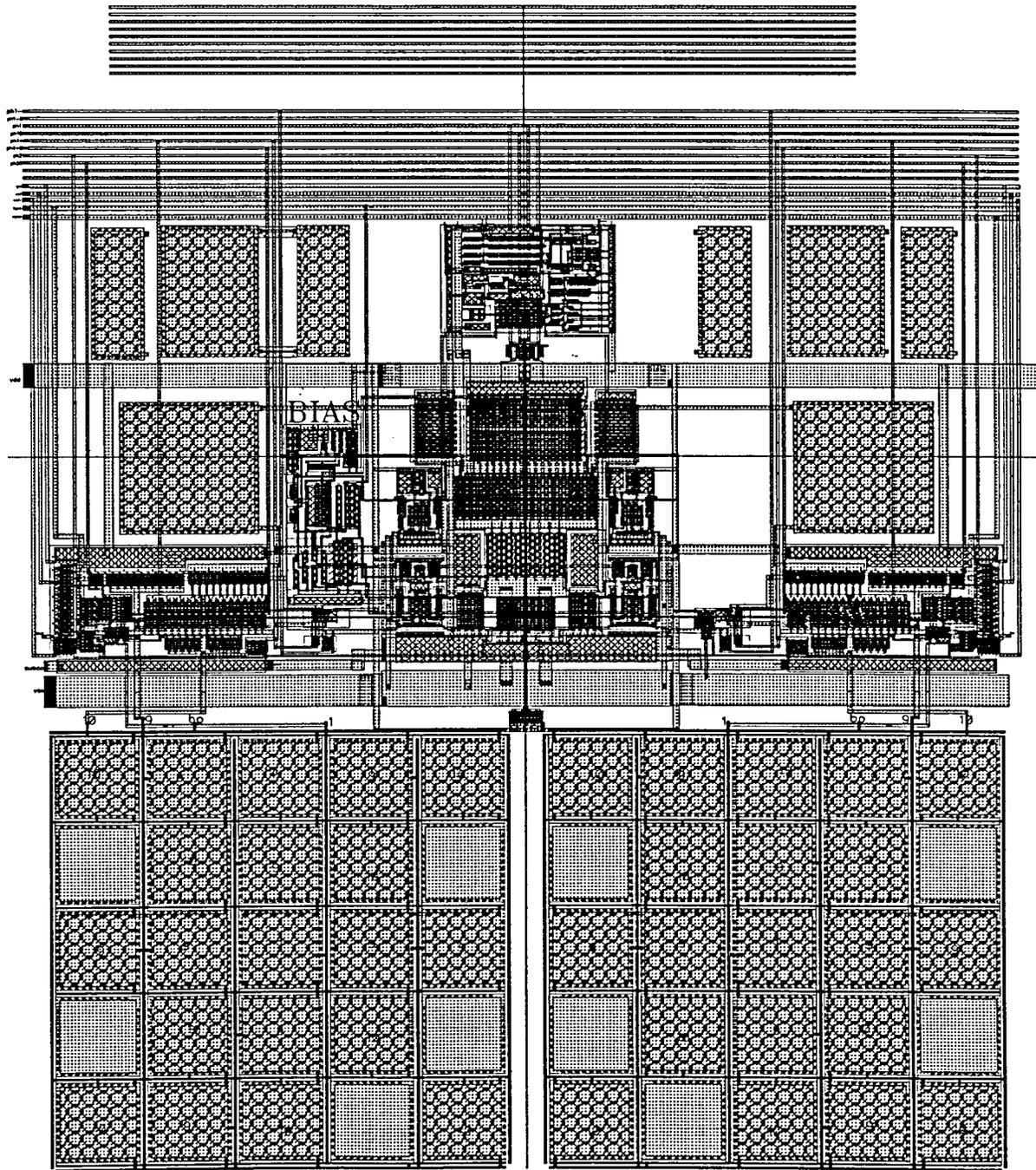


Figure 4.8 Layout of one stage

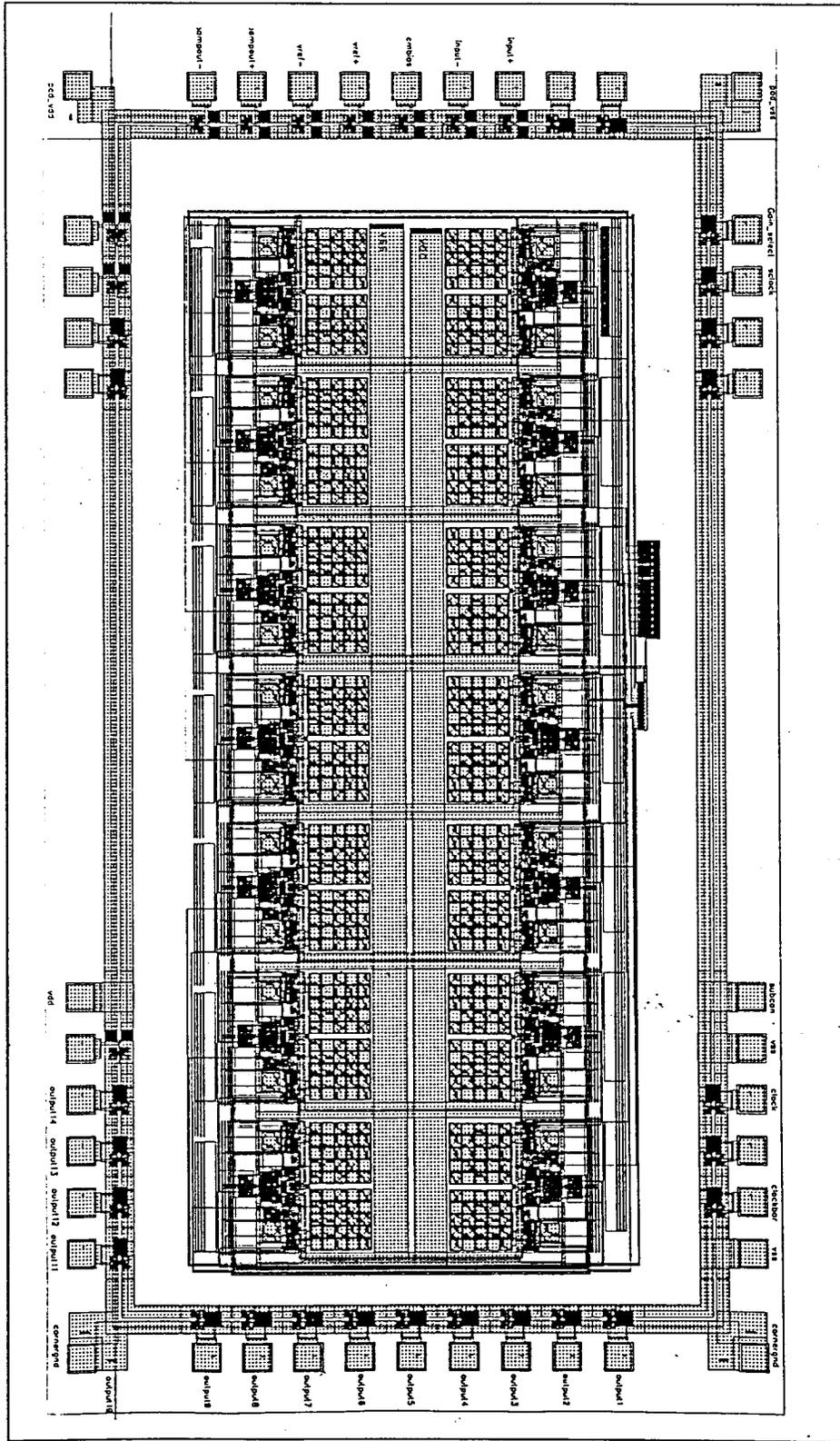


Figure 4.9 Layout of whole pipeline

### 4.3 I/O Signals And Off-chip Calibration

For the convenience of testing and off-chip digital calibration, I/O signals for each stage are listed in Table 4.2. For each additional stage, one additional digital output is needed.

Table 4.2 I/O signals for each stage

Power (Vdd, Vss, substrate )	3
Differential references	2
Gnd, Cmbias	2
Analog inputs and outputs (differential)	4
Digital input and output	2
Clocks	10
Calibration mode	1

Each stage of the pipelined ADC has two mode: normal conversion mode and calibration mode. MUXs are needed at the inputs of each stage. During calibration mode, the “calibration mode” of the cell will be set to “1”, and the MUXs will pass the input signals from the pads. During normal conversion mode, the “calibration mode” will be “0”, and the MUXs will pass the signals from the previous stage.

The digital self-calibration is performed off-chip for the flexibility of testing the algorithm. At one time during calibration, only one stage is being calibrated, all the rest stages are in normal conversion mode to measure the calibration constants  $S1$  and  $S2$ .  $S1 - S2$  of each stage will be stored in a 13-bit RAM.

To finish one calibration cycle for all 14 stages, 7.84us, i.e.  $2 \times 14 \times 14 \times 20\text{ns}$  is needed. Usually 30 calibration cycles are used to average the noise out. The total time needed for the off-line calibration is about 235us.

## 5 CONCLUSION AND FUTURE WORK

### 5.1 Conclusion

This thesis has discussed the architecture and implementation of a 12-bit 50M samples/s digitally self-calibrated analog-to-digital converter. The contributions of the author can be listed as following:

1) Proposed a cell architecture with a transfer characteristics being  $V_{out} = 1.9V_{in} \pm 0.95V_{ref}$ .

2) Designed and implemented the cell. The  $0.95V_{ref}$  was supplied off-chip. A capacitor array including “0.1C”, “0.9C” and “C” is used to improve the matching. The simulation results shows the settling time of the MDAC is 9ns with the 81dB DC gain of the OTA.

3) Overall system implementation including system timing, simulation and floorplanning.

The propotype ADC has been implemented in  $0.35 \mu\text{m}$  CMOS process.

### 5.2 Power Optimization

Power dissipation is becoming an increasingly important issue in the design of analog-to-digital converters because the popularity of the portable devices. The 12-bit 50Msamples/s pipelined ADC presented in the previous chapters consumes  $33 \times 14 = 462\text{mW}$  (33mW is the power for each stage as shown in Table 3.3, comparator power consump-

tion is negligible compared to MDAC) which may not be good enough for the low power application. As a result, reducing the power dissipation is an important direction for future work.

In this pipelined ADC, most of the power dissipation occurs in the operational transconductance amplifier. During the hold mode, the possible power saving may not be appreciable because the high speed application demands a large bias current for the OTA. During the sample mode, however, the OTA is nearly idle except the input nodes and the output nodes are all set to the common-mode voltage. We can probably save 25% of the power consumption if somehow the bias current of the amplifier can be reduced by 50% in the sample mode. The challenge is how to apply the current switching without affect the overall performance.

In addition, it is obvious that the performance of the first stage of the pipeline is most critical. Not only the multiplying ADC needs to be accurate to the full resolution of the converter, the tolerable  $KT/C$  noise also needs to be least since the equivalent input-referred noise contribution from the subsequent stages is attenuated by the interstage gain of all previous stages. As a result, the size of the sampling capacitors of the later stages can be smaller than the capacitance in the first stage. Because the sampling capacitors are the main loads for the OTA, the power dissipation of the OTA can be greatly reduced by properly scaling down the capacitance of all the capacitance in the pipeline.

### 5.3 Speed Optimization

Higher speed is required for future application such as wireless communication. Shooting for higher speed, interleaving techniques [Black80] may be applied.

The parallel pipelined ADC is one of the interleaving application. However, the hardware required increases proportionally to the speed. Another interleaving technique

which requires less hardware by sharing residue amplifiers and sub-ADC comparators between two time interleaving channels was proposed [Bright98]. It can be another direction of the future work.

Besides the two important design parameters discussed above, the clock generation circuits such as DLL may need to be developed for better control of the timing.

## APPENDIX TRANSISTOR SIZES

Table A.1 Folded-cascode parameters

M0, M1	426/0.4
M3, M4	262.4/0.4
M5, M6	117.6/0.4
M7, M8	116.8/0.4
M10, M11	400/0.4
M9	326.4/1

Table A.2 PMOS-boosting amplifier parameters

M0, M2	13.6/0.4
M1, M3	6/0.4
M4, M5	10.6/0.8
M6, M7	30/0.4
M8	15/0.4

Table A.3 NMOS-boosting amplifier parameters

M0, M3	19.8/0.4
M1, M2	10/0.4
M4, M5	10.4/0.8
M6, M7	30/0.4
M8	18.2/0.4

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